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LOW-INPUT-HARMONICS POWER SUPPLIES
BY: C HU, USC, BERKELEY

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NOSC CR 159
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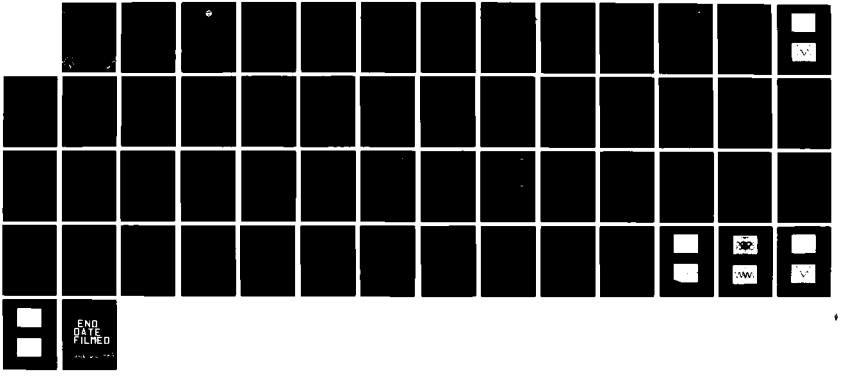

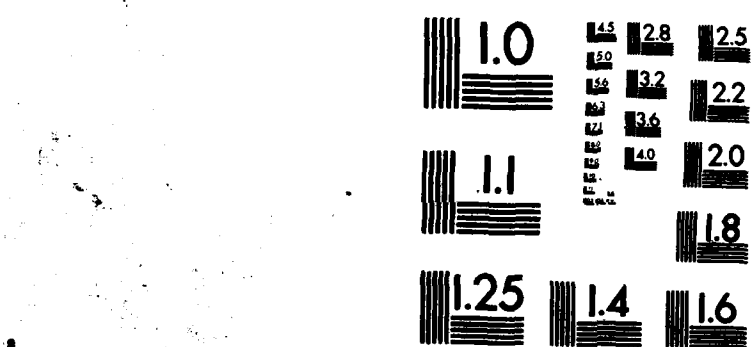

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Contractor Report 159

LOW-INPUT-HARMONICS POWER SUPPLIES

Prepared by
Chenming Hu
University of California, Berkeley
Contract: N66001-81-C-0538

October 1982

Final Report

Prepared for
Naval Ocean Systems Center
Code 5512

NAVAL OCEAN SYSTEMS CENTER
San Diego, California 92152

NAVAL OCEAN SYSTEMS CENTER, SAN DIEGO, CA 92152

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ADMINISTRATIVE INFORMATION

This work and final report were completed by University of California, Berkeley, California, under contract N66001-81-C-0538 for NOSC Code 5512 for the period ending October 1982.

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LJ Gray, Head
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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER NOSC Contractor Report 159 (CR 159)	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* LOW-INPUT-HARMONICS POWER SUPPLIES		5. TYPE OF REPORT & PERIOD COVERED Final Report 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Chenming Hu		8. CONTRACT OR GRANT NUMBER(s) N66001-81-C-0538
9. PERFORMING ORGANIZATION NAME AND ADDRESS University of California Berkeley, CA 94720		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Element: 62543N Project: XF43453401
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Ocean Systems Center San Diego, CA 92152		12. REPORT DATE October 1982 13. NUMBER OF PAGES 56
14. MONITORING AGENCY NAME & ADDRESS*(if different from Controlling Office)* Naval Electronic Systems Command Washington, DC 20360		15. SECURITY CLASS. *(of this report)* Unclassified 15a. DECLASSIFICATION/ DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

low-input-harmonics converter
harmonic currents

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

In this report the 3 objectives were successfully accomplished. They are (a) construction of a low-input-harmonics converter, (b) characterization of the input current harmonics and (c) theoretical analysis of the input harmonics and other performances of the novel converter.

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CONTENTS

ABSTRACT

This final report covers Phase I of the project. All three objectives have been successfully accomplished. They are (a) construction of a low-input-harmonics converter, (b) characterization of the input current harmonics, and (c) theoretical analysis of the input harmonics and other performances of the novel converter.

Specifically, it has been shown that the 3% harmonics requirement can be met without the use of low frequency filters or phase-shifting transformers.

This circuit can not perform ac to dc conversion. Pending continued funding of Phase II of this project, a 3-phase ac to dc power converter will be demonstrated. A new circuit having even lower input harmonics and much lower switching frequency noises than the circuit reported here will be constructed and characterized. Harmonics contents and stability of the power supply will be thoroughly studied.

I. INTRODUCTION

The operating principle of the low-input-harmonics power converter, its basic configuration and operation have been thoroughly discussed in the Interim Report. They are also summarized in a report entitled "Input-Harmonic-Free Frequency Converter" and attached here as the Appendix. The Appendix not only presents the experimantal and theoretical performance data of the converter, but also describes the filter design and device ratings. The following are highlights of the input harmonics results and supplements to the contents of the Appendix.

II. INPUT CURRENT HARMONICS

Figure 1 shows an example of the simulated input current spectrum. In the low frequency end of the spectrum there is one dominant peak at 60 Hz (normalized to 100%). Large harmonic currents appear around the switching frequency (25.9 kHz in this example). These high frequency harmonics can be filtered with small filters as in the case of conventional switching power supplies. Figure 2 shows the harmonic currents in an expanded scale. Clearly, the 3% harmonics can be satisfied without a filter.

Figure 3 shows the measured spectrum of the input current. The dominant peak is at 60 Hz. All other peaks are at least 36 dB (in power) lower or less than 1.5% of the fundamental. The rapid fall-off beyond 300 Hz is due to an LC filter with cut-off frequency at 300 Hz designed to eliminate the switching frequency ripples.

Figure 4 shows the same input current waveform in time domain.

III. AC TO DC CONVERSION

The prototype converter reported here can not perform ac to dc conversion because it contains no feedback circuit for maintaining constant output frequency and amplitude. Rather it is a general frequency changer with the output frequency being equal to the input frequency (f_i) minus an adjustable modulation frequency (f_m). For example, the output frequency under the conditions shown in Fig. 1 is $f_i - f_m = 60 - 180 = -120$ Hz.

A feedback circuit that will allow the demonstration of regulated dc power supply has been designed and partially assembled. The completion of the construction and testing depends on continued funding of this project.

IV. OTHER APPLICATIONS

While the low-input-harmonics characteristics and the application as a dc power supply are the emphasis and goal of this research project, the converter itself has many other unique attributes, which may lead to other useful applications.

- Conversion to variable amplitude variable frequency (including dc) output
- free of input and output harmonics without need for line filters
- unity power factor
- potentially smaller size and lighter weight due to the absence of rectifier, dc filter, and the input and output filters.

A list of potential applications:

. ac to dc power supply

. 60 Hz to 400 Hz (or 400 to 60) converter

. highly regulated AC supply

. power factor correction

. harmonic current sink (replacing tuned filters)

. dc to 10 kHz power generation for sonar or communication

V. NEW CONVERTER CONCEPT

A new low-harmonics converter concept has occurred to us. It has the same attributes as described in Section IV above -- only better. The circuit configuration is the same as shown in Fig. 1a in the Appendix. The switching pulse width modulation algorithm is changed so that the input current (and output voltage) does not change polarity in a switching sequence (period) in contrast to the waveforms shown in Fig.2 of the Appendix. The switching ripple and EMI are reduced by at least a factor of two. Even the low frequency harmonics are reduced. Figure 5 shows the simulated output voltage, V_0 and input current, I_i for the Venturini (V-) converter and the new (N-) converter. Clearly the new converter produces less harmonics in V_0 and I_i. (I_i harmonics are less obvious in Fig. 5 but are comparable to the V_0 harmonics.) This new converter will be developed and characterized if Phase II is funded.

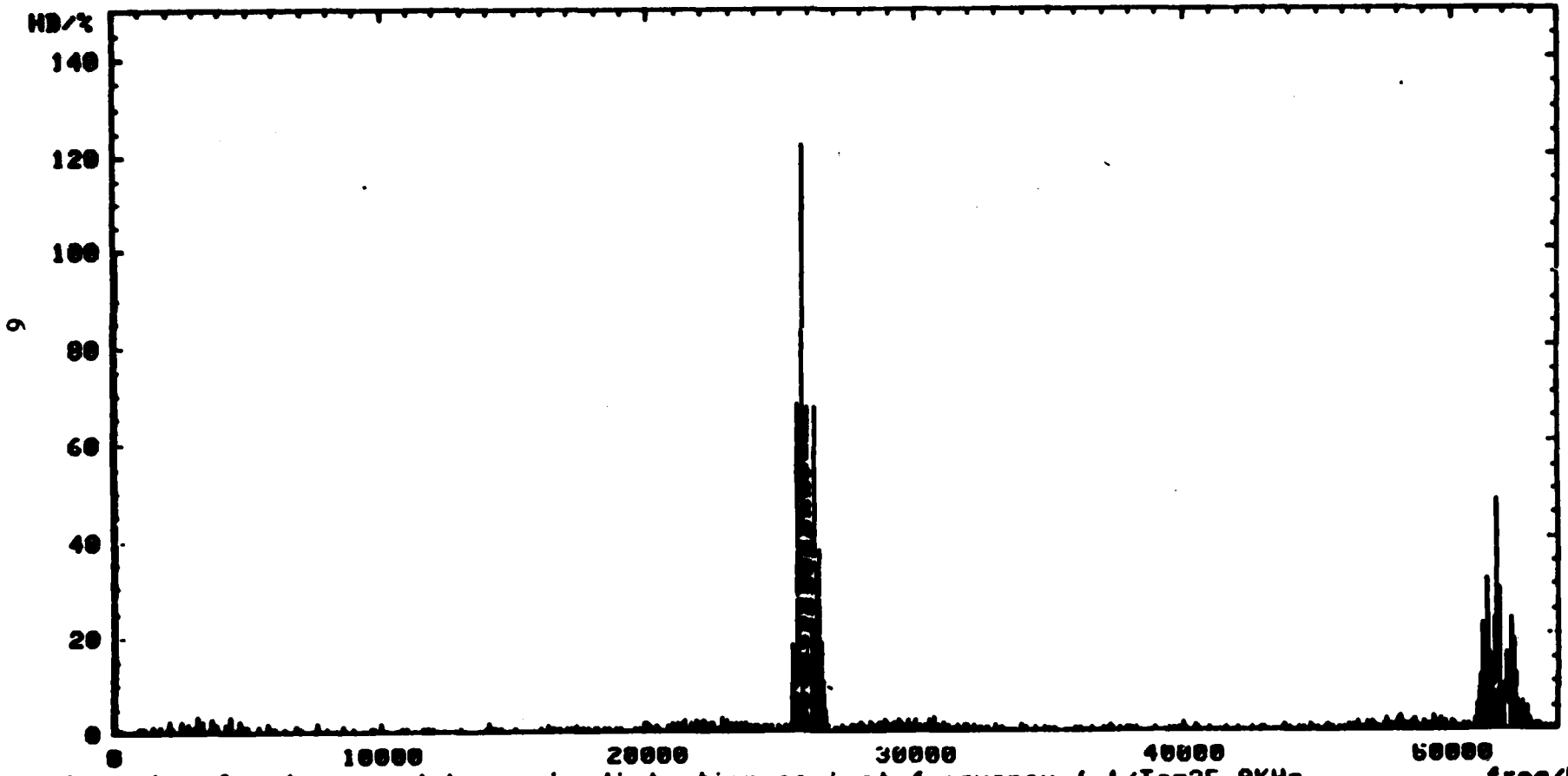


fig. 1 Input current harmonic distortion against frequency (1/Ts=25.9KHz, fi=60 Hz, fm= 180 Hz, m= 0.4)

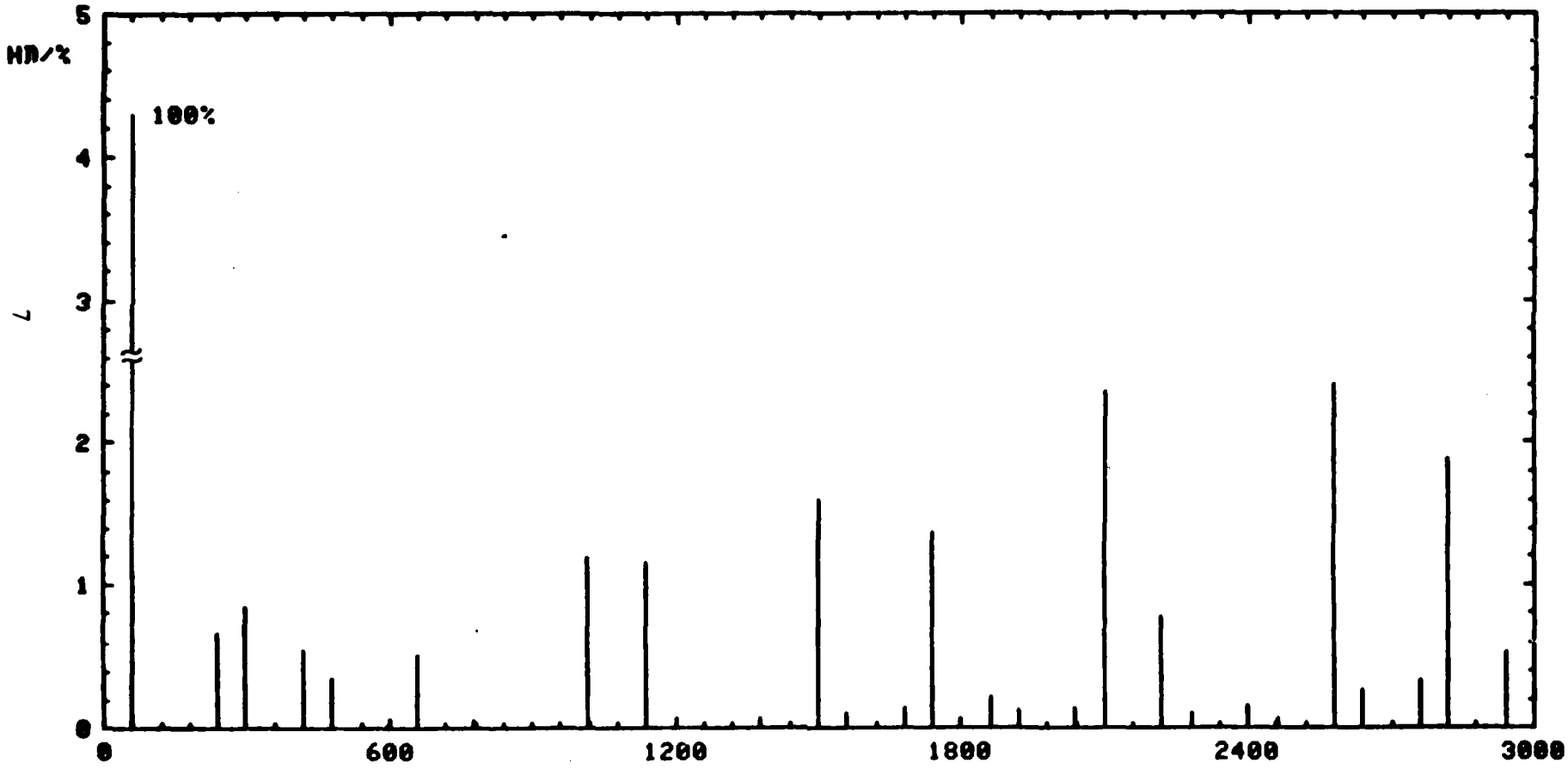


fig. 2 Normalized low-frequency components of the input current (1/Ts=25.9KHz, fi = 60 Hz, fm = 180 Hz, m = 0.4)

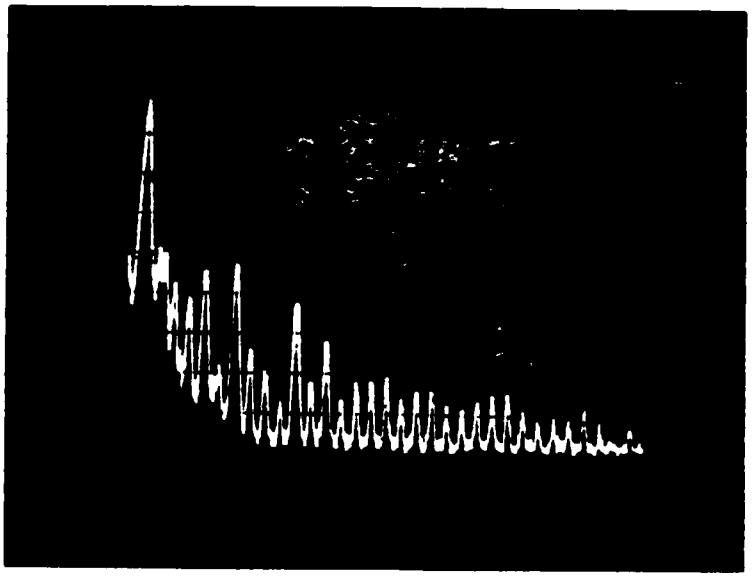


Fig. 3 Line current spectrum (10db/div, 200Hz/div).

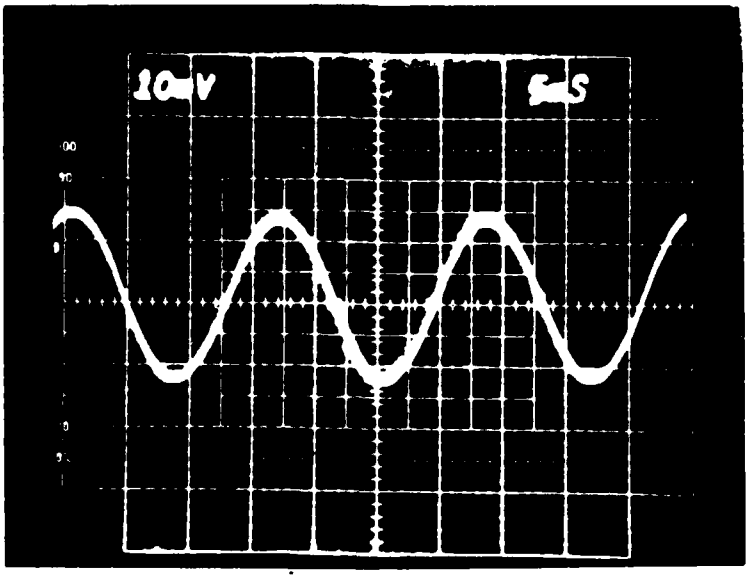
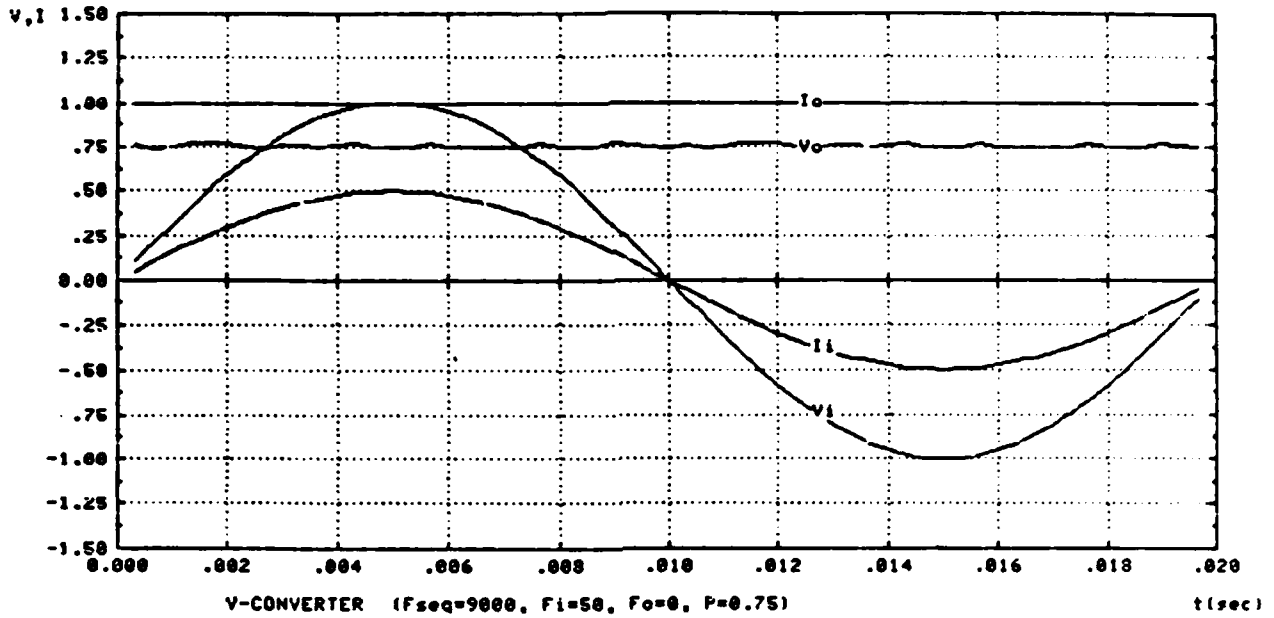


Fig. 4 Line current iin1 (25mA/div).


V,I 1.50
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1.00
.75
.50
.25
0.00
-.25
-.50
-.75
-1.00
-1.25
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Io
Vo
Ii
Vi
0.000
.002
.004
.006
.008
.010
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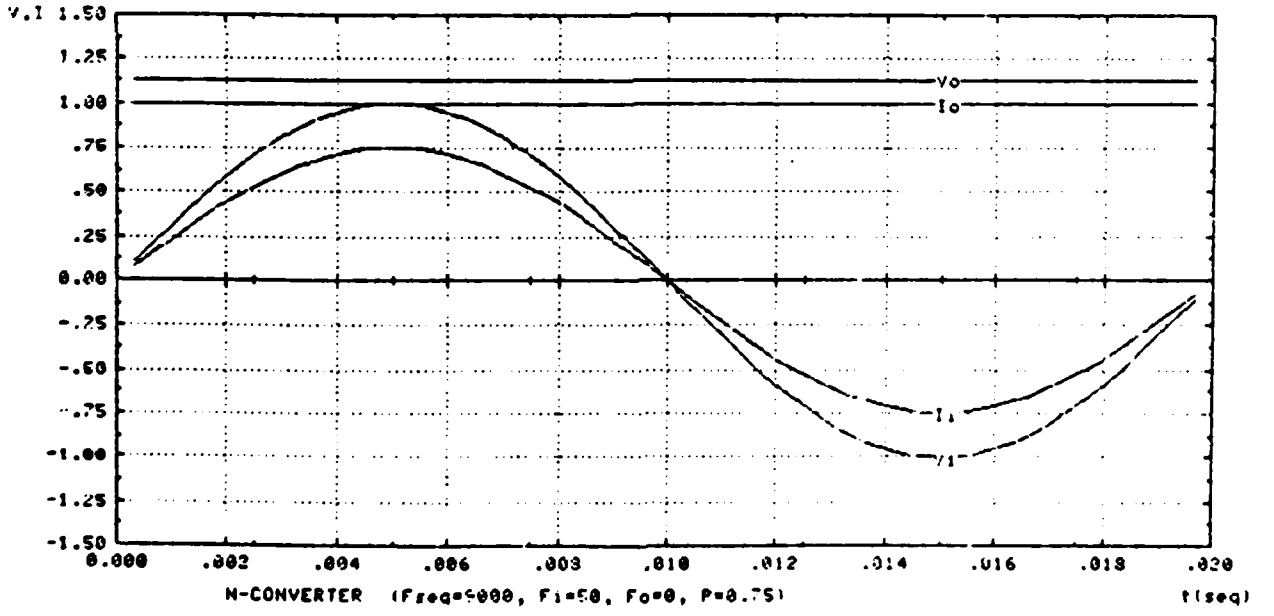
.014
.016
.018
.020
V-CONVERTER (Fseq=9000, Fi=50, Fo=0, P=0.75)
t(sec)


V,I 1.50
1.25
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-.25
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-.75
-1.00
-1.25
-1.50
Vo
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Ii
Vi
0.000
.002
.004
.006
.008
.010
.012
.014
.016
.018
.020
N-CONVERTER (Fseq=9000, Fi=50, Fo=0, P=0.75)
t(seq)

Fig. 5

APPENDIX I

Input-Harmonic Free Frequency Converter

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ABSTRACT

The implementation of a recently proposed ac frequency changer is described. Interesting features of the converter include sinusoidal input and output waveforms, bidirectionality and variable output voltage amplitude and frequency. This paper describes the pulse-modulation control circuit, filter design considerations, device rating and protection. Measured input and output waveforms are presented.

Input-Harmonic Free Frequency Converter

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1. Introduction

The new converter investigated is based on the concept of high- frequency synthesis of slow-varying waveforms. The converter connects three input lines to three output lines through nine switches (fig.1). The switches are closed and opened according to a specific pulse-width modulation algorithm derived by Alesina and Venturini [1]. Because of high frequency-switching, small filters can be used. In addition to the size and weight advantages inherent in switching converters, this modulation algorithm provides several other interesting advantages. These include sinusoidal input currents and output voltages, independent controls over output amplitude and frequency In this converter, the switch rms current may be considerably larger than the input or output currents. An analysis of the switch current will be presented. If the switching pulses φ_1, φ_2 and φ_3 overlap due to finite switching time of the solid-state devices, sizable transient current exceeding the current rating of the switching devices may result (fig. 6(c)). On the other hand, due to inductive loads, nonoverlapping switching pulses may cause destructive voltage overshoots.

The overlap/underlap dilemma is circumvented by restricting current spikes with protection circuit. Finally voltage and current

waveforms of the complete converter are presented.

2. Pulse-width Modulation Algorithm

The control law for the switches used here is a simplified version of the generalized algorithm given in [1]. In this simplified algorithm, the on-times t_{w1}, t_{w2} and t_{w3} of the command pulses φ_1, φ_2 and φ_3 (fig.1) are given by

$$t_{w1}(kTs) = \frac{T_s}{3}[1+2m\cos(\omega_m k T_s)] \tag{1a}$$

$$t_{w2}(kTs) = \frac{T_s}{3}[1+2m\cos(\omega_m k T_s + \frac{2\pi}{3})] \tag{1b}$$

$$t_{w3}(kTs) = \frac{T_s}{3}[1+2m\cos(\omega_m k T_s - \frac{2\pi}{3})] \tag{1c}$$

If the input sinusoidal voltages take the form

$$v_{i1}(t) = V_i \sin(\omega_i t) \tag{2a}$$

$$v_{i2}(t) = V_i \sin(\omega_i t + \frac{2\pi}{3}) \tag{2b}$$

$$v_{i3}(t) = V_i \sin(\omega_i t - \frac{2\pi}{3}) \tag{2c}$$

then the time average value of the staircase-like output $v_{o1}(t)$ in the interval [k T_s, (k+1) T_s) is given by

$$v_{o1ave}(kTs) = \frac{1}{T_s}\int_{kT_s}^{(k+1)T_s} v_{o1}(t)dt$$

$$\approx \frac{1}{T_s}[v_{i1}(kTs)t_{w1}+v_{i2}(kTs)t_{w2}+v_{i3}(kTs)t_{w3}]$$

$$= mV_i \sin(\omega_o kT_s) \tag{3}$$

where T_s is small and $\omega_o = \omega_i - \omega_m$.

Similarly it can be shown that

$$v_{o2ave}(kTs) = mV_i \sin(\omega_o kT_s + \frac{2\pi}{3}) \tag{4}$$

$$v_{o3ave}(kTs) = mV_i \sin(\omega_o kT_s - \frac{2\pi}{3}) \tag{5}$$

Thus ω_m is the difference between the input and output frequencies. In addition, the output voltage amplitude is m times that of the input. It is important to emphasize that (3), (4) and (5) represent the primary low frequency components of the outputs $v_{o1}(t)$, $v_{o2}(t)$ and $v_{o3}(t)$, whereas in the absence of filter the instantaneous output voltages are staircase-like.

For linear time-invariant loads, the output current waveforms are sinusoidal. Analogous to the arguments given for the output voltages, the primary low-frequency component of the instantaneous input current waveforms occurs at the input frequency ω_i and has an amplitude of

$$I_{iave} = mI_o \tag{6}$$

where I_o is the amplitude of the output currents.

Typical unfiltered output voltage and input current waveforms are shown in fig.2.

Unfiltered output voltage spectrum is given in [1]. The normalized Fourier spectra for the input current are shown in fig.3. These spectra suggest that with large m and small T_s, the conversion algorithm is capable of providing low-harmonic input current up to the 30th - 40th

harmonics. Harmonic current components at higher frequencies can be easily eliminated with proper filtering. This type of converter is therefore characterized by sinusoidal input and output waveforms, independent controls over frequency and amplitude. Timing error and input imbalance, as expected, introduce subharmonics at frequencies lower than 60 Hz (fig 3.(f)-(h)). Therefore the accuracy of the switching pulses play an important role in suppressing current harmonics.

3. Prototype Power Converter

3.1. Control Unit

The overall block diagram of the prototype converter is shown in fig.4. The switching matrix consists of nine power MOSFET bidirectional switches (fig.5). The command pulses φ_1, φ_2 and φ_3 are generated by means of a digital control unit whose block diagram is given in fig. 6(a). At the start of the operation, the accumulator is reset. Its content is then increased by ω_m at a rate of T_s^{-1}. The update pulse for the accumulator is taken from the borrow output b_1 of the counter 01. The normally high b_1 line goes low only when the counter 01 reaches zero. In order to generate a balanced three-phase modulating function, an EPROM is used to store the three-phase cosine table. The EPROM is divided into eight sections. In each section, a cosine table is stored (fig.6(b)). The memory is addressed by eleven address lines. The three most significant address lines are provided by (i) the sign bit of ω_m and (ii) the state of the counter status flip-flops. The sign bit of ω_m determines the page of the memory to be addressed. The cosine table stored in the two pages are the results of the following trigonometric identities

$$\cos(-x) = \cos x$$

$$\cos(-x + \frac{2\pi}{3}) = \cos(x + \frac{4\pi}{3})$$

$$\cos(-x + \frac{4\pi}{3}) = \cos(x + \frac{2\pi}{3})$$

The counter status flip-flops are initialized to 001. While counter 00 counts down to zero, the number to be loaded into next counter (01) is being fetched, multiplied and loaded into the other two counters. As the counter 00 reaches zero, its borrow pulse b_0 causes the counter status flip-flop to transit from the state 001 to the state 010. The resulting memory address line changes allow another section of the memory to be addressed. The interval $t_{w2}(kTs)$ permits $t_{w3}(kTs)$ to be generated before the counter 01 reaches zero.

3.2. Switching Frequency Filters

The quasi-square wave output (fig.2) may be acceptable in certain applications such as motor drive. In general, the power converter requires output filter to smooth out the output waveforms. In addition, input filter is necessary to provide a smooth current waveform.

Fig.7 illustrates one possible filter configuration. Although a balanced system will be used in practice, the filters for one phase are illustrated for simplicity. Assuming sinusoidal driving voltage sources, the instantaneous output $v_o(t)$ is a quasi-square wave. In addition, due to the inductor L_o, its current cannot undergo abrupt changes. Because of the switching algorithm and the continuity of the output inductor current, the instantaneous input current is also staircase-like (fig.2(b)). Therefore C_i serves as a harmonic current sink that removes the unwanted

switching harmonics from the line current.

>From the Fourier spectra given in fig.3, it is seen that the filter corner frequency should be placed between $\frac{2\pi}{\omega_o}$ and T_s^{-1} for the maximum blocking at switching frequencies and the least attenuation around $\frac{2\pi}{\omega_o}$.

The output of a sinusoidal synthesizer should be low in switching ripples and should have low harmonic distortions caused by the unwanted components near ω_o. Now referring to fig.7, it is obvious that the instantaneous output inductor current is the integral of the instantaneous inductor voltage (fig.8(a)). If the switching frequency T_s^{-1} is much higher than the input and output frequencies, then

$$\Delta i_{L_{o1}} = \frac{t_{w1}(kTs)}{L_o}[v_{i1}(kTs) - v_R(kTs)]$$

$$= \frac{V_i T_s}{3L_o}[\sin(k\omega_i Ts) - m'\sin(k\omega_o T_s + \psi)][1 + 2m\cos(k\omega_m Ts)] \quad (7)$$

$$\Delta i_{L_{o2}} = \frac{V_i T_s}{3L_o}[\sin(k\omega_i T_s + \frac{2\pi}{3}) - m'\sin(k\omega_o T_s + \psi)]$$

$$[1 + 2m\cos(k\omega_m T_s + \frac{2\pi}{3})] \quad (8)$$

$$\Delta i_{L_{o3}} = \frac{V_i T_s}{3L_o}[\sin(k\omega_i T_s - \frac{2\pi}{3}) - m'\sin(k\omega_o T_s + \psi)]$$

$$[1 + 2m\cos(k\omega_m T_s - \frac{2\pi}{3})] \quad (9)$$

where the load voltage is assumed to take the form

$$v_R(t) = V_o\sin(\omega_o t + \psi)$$

$$= \frac{m V_i \sin(\omega_o t + \psi)}{\sqrt{(1 - C_o L_o \omega_o^2)^2 + \left(\frac{\omega_o L_o}{R_L}\right)^2}}$$

$$= m' V_i \sin(\omega_o t + \psi) \tag{10}$$

Both geometric consideration and numerical computation of (7) show that the maximum current ramp within an on-interval t_{on} is

$$\Delta i_{L_o \max} = \frac{0.43 V_i T_s}{L_o} \tag{11}$$

for all ω_i, ω_m, ψ and $0 < m,m' < 0.5$.

If the specified maximum allowable peak-to-peak output inductor current ripple is to be $100\delta_1$ % of I_o, then L_o is chosen according to

$$\Delta i_{L_o \max} < \delta_1 I_o$$

or

$$L_o > \frac{0.43 V_i T_s}{\delta_1 I_o} \tag{12}$$

Under the assumption that

$$T_s^{-1} >> \max(f_o, f_i) \tag{13}$$

the inductor current waveform i_{L_o} is a linear ramp during t_{on} $(n = 1, 2, 3)$. An interesting consequence is that there is no net current change during any switching period T_s, i.e.,

$$\Delta i_{L_{o1}} + \Delta i_{L_{o2}} + \Delta i_{L_{o3}} = 0 \tag{14}$$

Equation (14) should be remembered as an approximation resulting from the assumption (13). Referring to fig.7, at any instant, the sum of the currents in L_o and C_o must equal the load current. In the extreme case where L_o is chosen to provide a ripple-free inductor current, there can be no harmonic currents at frequencies other than f_o flowing into or out of C_o. Since the average inductor current during $[kTs,(k+1)T_s)$ constitutes the sinusoidal load current (fig.8(b)). The charge packets above and below $I_{L_{ave}}(kTs)$ flow into C_o producing ripple voltages (fig.8(c)). To select C_o for specified maximum output ripples, it is necessary to know the maximum size of the charge packet. Numerical simulation results are given in fig. 9 where R_p denotes the absolute value of charge packet normalized to $\frac{V_i T_s^2}{L_o}$. >From fig.9(c),

$$\Delta v_{R_{max}} = \frac{0.0551 V_i T_s^2}{L_o C_o} \tag{15}$$

If the maximum allowable output voltage ripple is to be $100\delta_2$ % of V_o, then C_o should be chosen according to

$$\frac{0.0551 V_i T_s^2}{L_o C_o} < \delta_2 V_o$$

or

$$C_o > \frac{0.0551 T_s^2}{m' \delta_2 L_o} \tag{16}$$

where the relation $V_o = m' V_i$ has been used.

If the input capacitor voltage and the input current ripples are to be within $100\delta_3$ % of V_i and $100\delta_4$ % of the input current amplitude I_i

respectively, then by duality argument C_i and L_i should be chosen according to

$$C_i > \frac{0.43 I_o T_s}{\delta_3 V_i} \tag{17}$$

and

$$L_i > \frac{0.0551 I_o T_s^2}{\delta_4 I_i C_i} \tag{18}$$

4. Device Current Rating

For power applications, the maximum voltage, current and power ratings of the FET switches should not be exceeded. To prevent excessive device power dissipation, it is necessary to restrict transient current spikes and limit the steady-state switch current. With a properly designed output filter, the load voltage $v_R(t)$ is sinusoidal and has an amplitude of $m' V_i$. If L_o is chosen to provide a smooth inductor current $i_{L_o}(t)$, then the load current $i_R(t)$ will also be sinusoidal with an amplitude of $I_o = \frac{m' V_i}{R_L}$. If the current flowing through the switch S_{11} is denoted by $i_{S_{11}}(t)$, then from (fig.1(a))

$$i_{R1}(t) = i_{S_{11}}(t) + i_{S_{21}}(t) + i_{S_{31}}(t) \tag{19}$$

Squaring both sides of (19) and noting that φ_1, φ_2 and φ_3 are mutually disjoint, we have

$$i_{R1}^2(t) = i_{S_{11}}^2(t) + i_{S_{21}}^2(t) + i_{S_{31}}^2(t) \tag{20}$$

So

$$\langle i_{R1}^2(t)\rangle = \langle i_{S11}^2(t)\rangle + \langle i_{S21}^2(t)\rangle + \langle i_{S31}^2(t)\rangle \quad (21)$$

Furthermore due to symmetry,

$$\langle i_{S11}^2(t)\rangle = \langle i_{S21}^2(t)\rangle = \langle i_{S31}^2(t)\rangle \quad (22)$$

Therefore the rms current flowing through each power switch is

$$\sqrt{\langle i_{Sij}^2(t)\rangle} = \sqrt{\frac{\langle i_{Rj}^2(t)\rangle}{3}} \quad (23)$$

for i, j = 1, 2 and 3.

For ac to ac conversion,

$$\sqrt{\langle i_{Sij}^2(t)\rangle} = \frac{I_o}{\sqrt{6}} \quad (24)$$

i, j = 1, 2 and 3.

For ac tc dc conversion,

$$\sqrt{\langle i_{Sij}^2(t)\rangle} = \frac{I_o}{\sqrt{3}} \quad (25)$$

i, j = 1, 2 and 3.

5. Device Protection

5.1. Limiting Switch Transient Current

It was mentioned previously that overlaps among φ_1, φ_2 and φ_3 resulted in spike current (fig. 6(c)).

Parallel RL circuits placed between C_i and the switching matrix (fig. 10) can reduce current spikes without introducing excessive loss. If the time constant $\frac{L_s}{R_s}$ is larger than the switching time of the MOS power FET's, R_s will be incorporated into the otherwise shorted path between two line sources, thereby preventing large current from flowing through the power devices during overlap transient. After transient settles, L_s provides a low-impedance path without degrading converter efficiency.

The maximum transient current $i_{S_{11max}}$ flowing through S_{11} can be found by referring to the control pulse φ_1 in fig.11 and the three- phase short circuit (fig.12) so formed during conduction exchange from the group $\{S_{11}, S_{22}, S_{33}\}$ to $\{S_{21}, S_{32}, S_{13}\}$. While S_{11}, S_{22} and S_{33} are closed $(t_0<t<t_1)$, the inductor L_{s1} carries the current $i_{L_{o1}}(t)$. Since inductor current cannot undergo abrupt changes, L_{s1} still carries $i_{L_{o1}}(t)$ immediately after t_1. If the on-resistance of the power devices is neglected, the voltage across the $R_s L_s$ combination is $v_{i1}(t)$ with a maximum value of V_i. Therefore in this interval

$$i_{s1}(t) = i_{L_{o1}}(t) + \frac{v_{i1}(t)}{R_{s1}} \tag{26}$$

Also

$$i_{S_{11}}(t) = \frac{i_{s1}(t)}{\sqrt{3}} \tag{27}$$

The maximum value of $i_{S_{11}}(t)$ can be easily found from the phasor diagram (fig.13) where $\vartheta(t)$ represents the angle between the two rotating vectors at time t. $\vartheta(t)$ is determined by the sizes of the output filter elements. The switch current reaches its maximum transient value when both vectors fall on the positive axes, i.e.

$$i_{S_{11max}} = \frac{V_i}{\sqrt{3}}\left[\frac{m'}{R_L}+\frac{1}{R_{s1}}\right] \tag{28}$$

$i_{S_{11max}}$ must be less than the maximum current rating I_{dm} of the MOSFET. So

$$R_s \geq \frac{V_i R_L}{\sqrt{3} I_{dm} R_L - m' V_i} \tag{29}$$

5.2. Limiting switch transient voltage

If switching were ideal, the maximum voltage across any FET switch would be just the amplitude of $v_{i1}(t)-v_{i2}(t)$. However, in practice the switch voltage can reach a higher momentary value during transient. Refer to fig.11 and consider the moment when the conduction exchange from the group $\{ S_{11}, S_{22}, S_{33} \}$ to $\{ S_{21}, S_{32}, S_{13} \}$ is just completed. Since the currents in the inductors cannot undergo instantaneous changes, L_{s1}, L_{s2} and L_{s3} carry $i_{L_{o1}}$, $i_{L_{o2}}$ and $i_{L_{o3}}$ respectively. Furthermore $i_{s1}=i_{L_{o3}}$, $i_{s2}=i_{L_{o1}}$ and $i_{s3}=i_{L_{o2}}$ due to current steering action associated with conduction exchange.

Summing voltages around the loop $v_{i1}-R_{s1}-S_{11}-S_{21}-R_{s2}-v_{i2}$ at this moment, it is found that

$$v_{i1}(t)+R_{s1}(i_{L_{o1}}(t)-i_{L_{o3}}(t))+v_{S_{11}}(t)$$

$$= R_{s2}(i_{L_{o2}}(t)-i_{L_{o1}}(t))+v_{i2}(t) \tag{30}$$

where $R_{s1}=R_{s2}=R_s$ and $v_{S_{11}}(t)$ denotes the voltage across S_{11}.

By Kirchhoff's current law,

$$i_{L_{o1}} = -(i_{L_{o2}}+i_{L_{o3}}) \tag{31}$$

Using (31) in (30) and rearranging,

$$v_{S_{11}}(t) = [v_{i1}(t)-v_{i2}(t)]-3i_{L_{o1}}(t)R_s \tag{32}$$

Following similar argument given above for $i_{S_{11max}}$, the absolute maximum transient value of $v_{S_{11}}(t)$ is

$$v_{S_{11max}} = \sqrt{3}V_i + \frac{3m'V_iR_s}{R_L} \tag{33}$$

where $i_{L_{o1}}(t)$ is assumed to be sinusoidal with an amplitude of $\frac{m'V_i}{R_L}$.

$v_{S_{11max}}$ should not exceed the maximum voltage rating of the MOS power FET at the current level $\frac{m'V_i}{R_L}$. Therefore

$$\sqrt{3}V_i + \frac{3m'V_iR_s}{R_L} < V_{DSm} \tag{34}$$

or

$$R_s < \frac{V_{DSm}-\sqrt{3}V_i}{3m'V_i} \tag{35}$$

5.3. Snubber Circuit

Because of deliberate switching overlap, there is no voltage overshoot due to the inductive loads. However experimental waveform for $v_x(t)$ (fig.14(a)) still indicated considerable overshoot due to damped sinusoidal transient. The frequency f_d of the damped sinusoid seems to indicate that overshoot is caused by the transient response of a parasitic RLC circuit. This was later verified by placing a small test capacitor C_t immediately after the switching matrix (fig.15) to modify f_d. The resulting decrease in f_d also allowed the values of the lumped parasitic inductance L_l and capacitance C_l to be calculated. The equivalent parasitic RLC circuit thus obtained is shown in fig.16.

The damping constant α_1 due to R_s can be found from the characteristic equation

$$s^2+s\frac{R_s}{L_l}+\frac{1}{L_l C_l}=0 \tag{36}$$

to be

$$\alpha_1 = \frac{R_s}{2L_l} \tag{37}$$

In order to reduce voltage overshoot, it is necessary to increase the effect of damping. However increasing R_s may not be desirable as can be seen from (35). As an alternative, a damping resistor R_p can be placed across the switching matrix output (fig.16). In order to prevent R_p from interfering steady-state operation, Cp is placed in series with R_p (fig.10) so that R_p is incorporated only during switching transient. The characteristic equation for the circuit in fig.16 can be shown as

$$s^2+s\left(\frac{R_s}{L_i}+\frac{1}{C_i R_p}\right)+\frac{1}{C_i L_i}\left(1+\frac{R_s}{R_p}\right) = 0 \qquad (38)$$

where the effective damping constant $\alpha_2 = \frac{1}{2}\left(\frac{R_s}{L_i}+\frac{1}{C_i R_p}\right)$.

The effect of damping ($Rp = 300\Omega$) on the voltage overshoot can be seen by comparing fig.14(a) with fig.14(b).

6. Experimental Results

The input and output waveforms of the prototype converter (fig.10) are shown in fig. 17. Comparison between the unfiltered and filtered waveforms can be made from fig. 17(a)-(d). The peculiar form of the unfiltered waveforms is due to the fact that the three-phase input voltages and output currents are chopped during conversion. The sizing of the filters were calculated using (12), (16), (17) and (18). The filtered output voltage (fig.17(b)) and the input current (fig.17(d)) appeared to be free of low-frequency ripples. This observation was again confirmed by their spectra (fig 17(e) and (f)).

Conclusion

A new power conversion algorithm was implemented. The sizing of the input and output filters, the device ratings and protection are analyzed. A prototype converter was built and tested. The converter converts ac and dc inputs to variable frequency- amplitude ac power with sinusoidal input and output waveforms.

Referenc

[1] A. Alesina and M. Venturini, "Solid-State Power Conversion: A Fourier Analysis Approach to Generalized Transformer Synthesis," IEEE Trans. CAS, vol. CAS-28, pp 319-330, no.4, Apr. 1981.

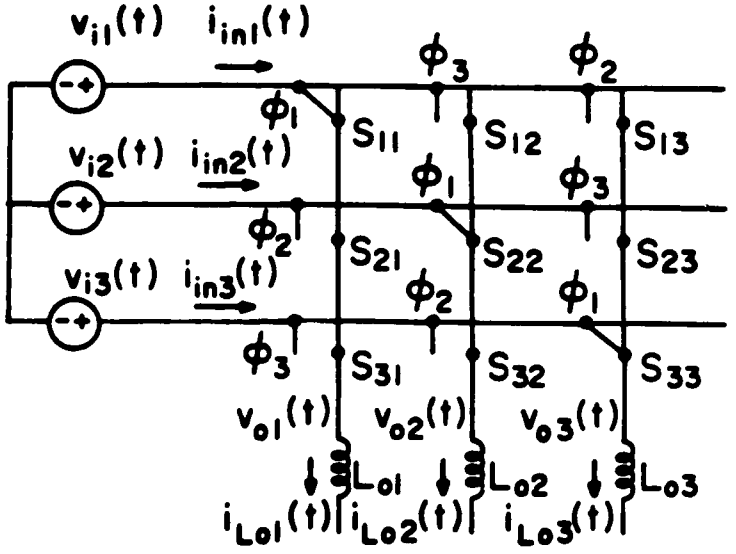

Fig. 1(a) General structure of a three-input, three-output high frequency synthesis converter

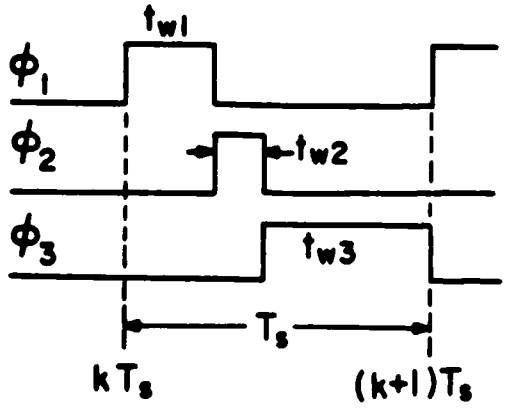

Fig. 1(b) Typical command pulses generated according to the algorithm proposed by Alesina and Venturini. The pulse width tw1 of ϕ1 is itself modulated by a sinusoid with angular frequency wm. Amplitude of the output is controlled by the index of modulation m.

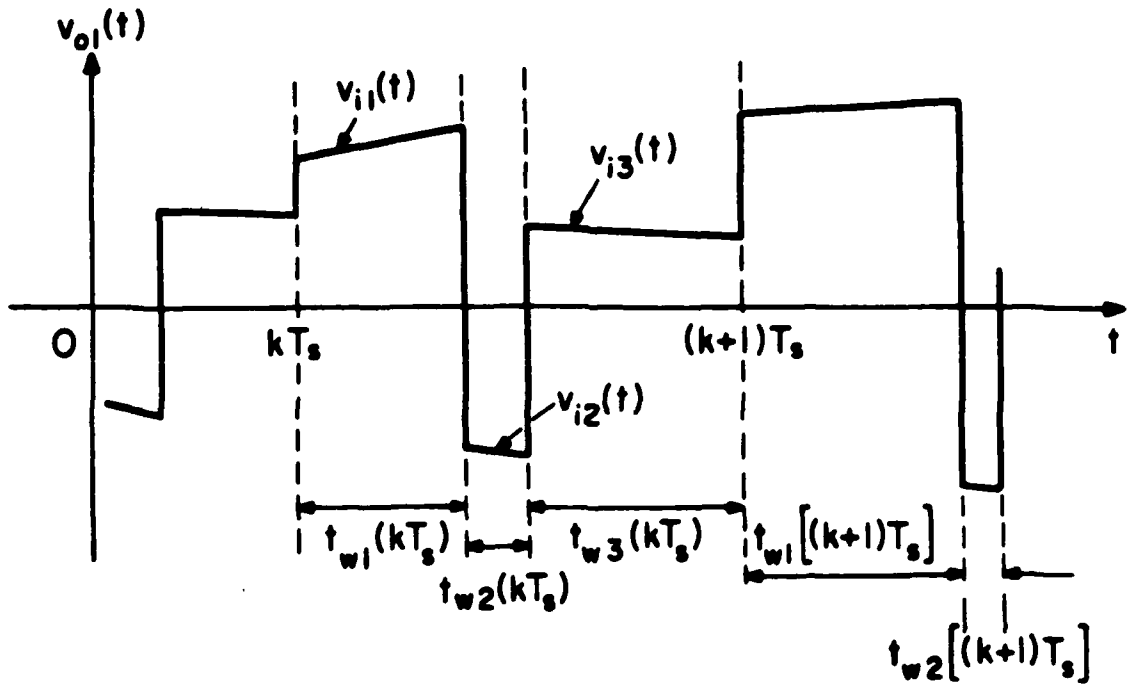

Fig. 2(a) Typical instantaneous output voltage waveform before filtering.

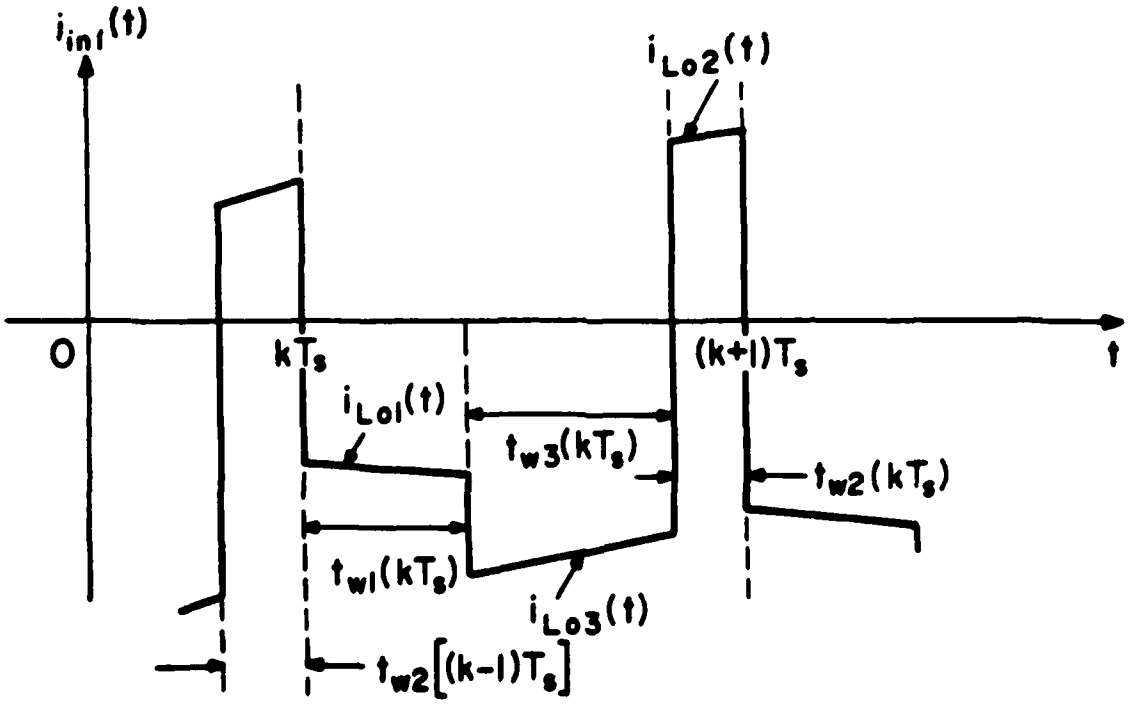

Fig. 2(b) Typical instantaneous input current waveform without filtering.

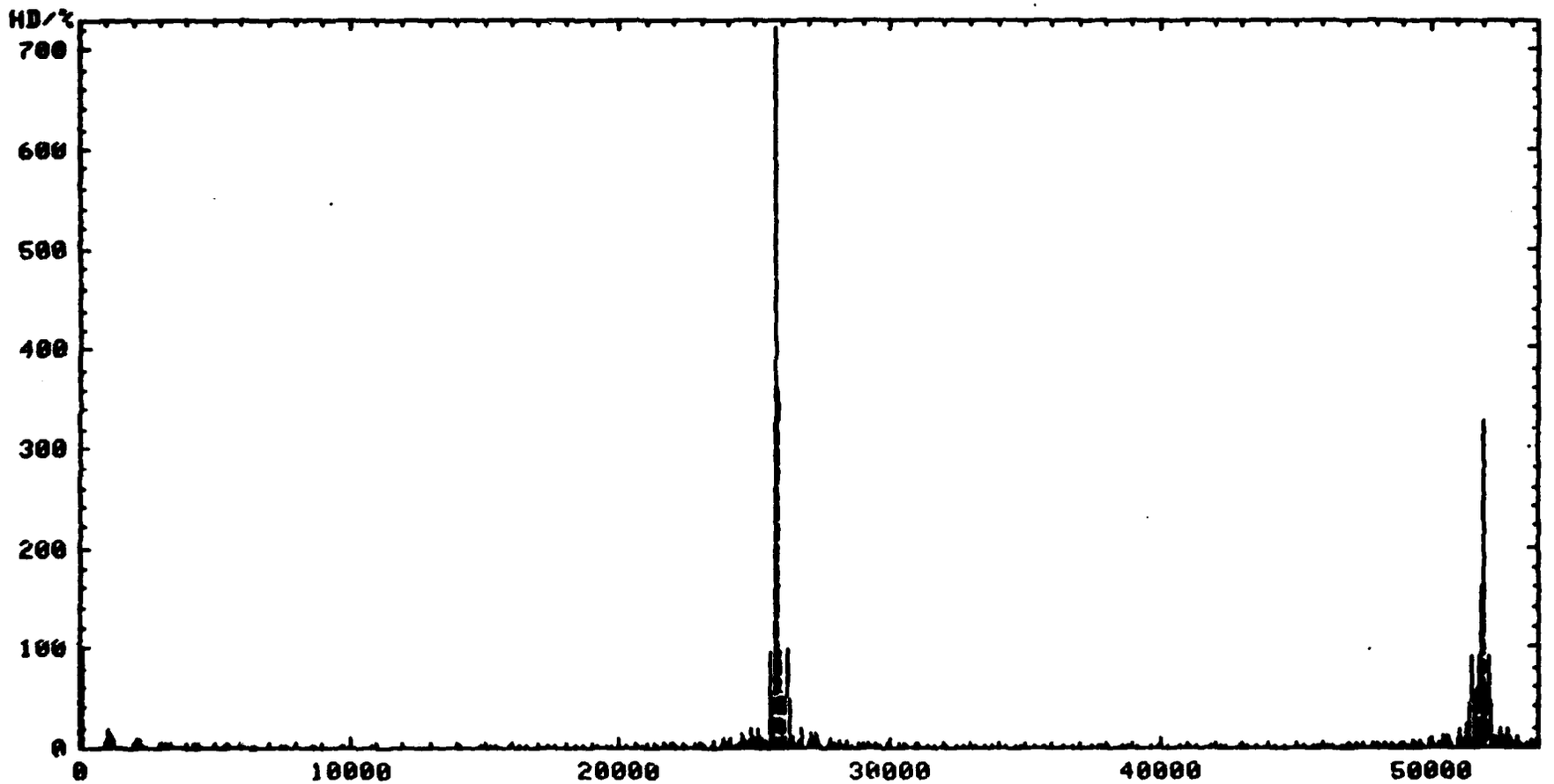

fig. 3(a) Input current harmonic distortion against frequency (1/Ts= 25.9KHz, fi= 60Hz, fm= 180Hz, m= 0.1)

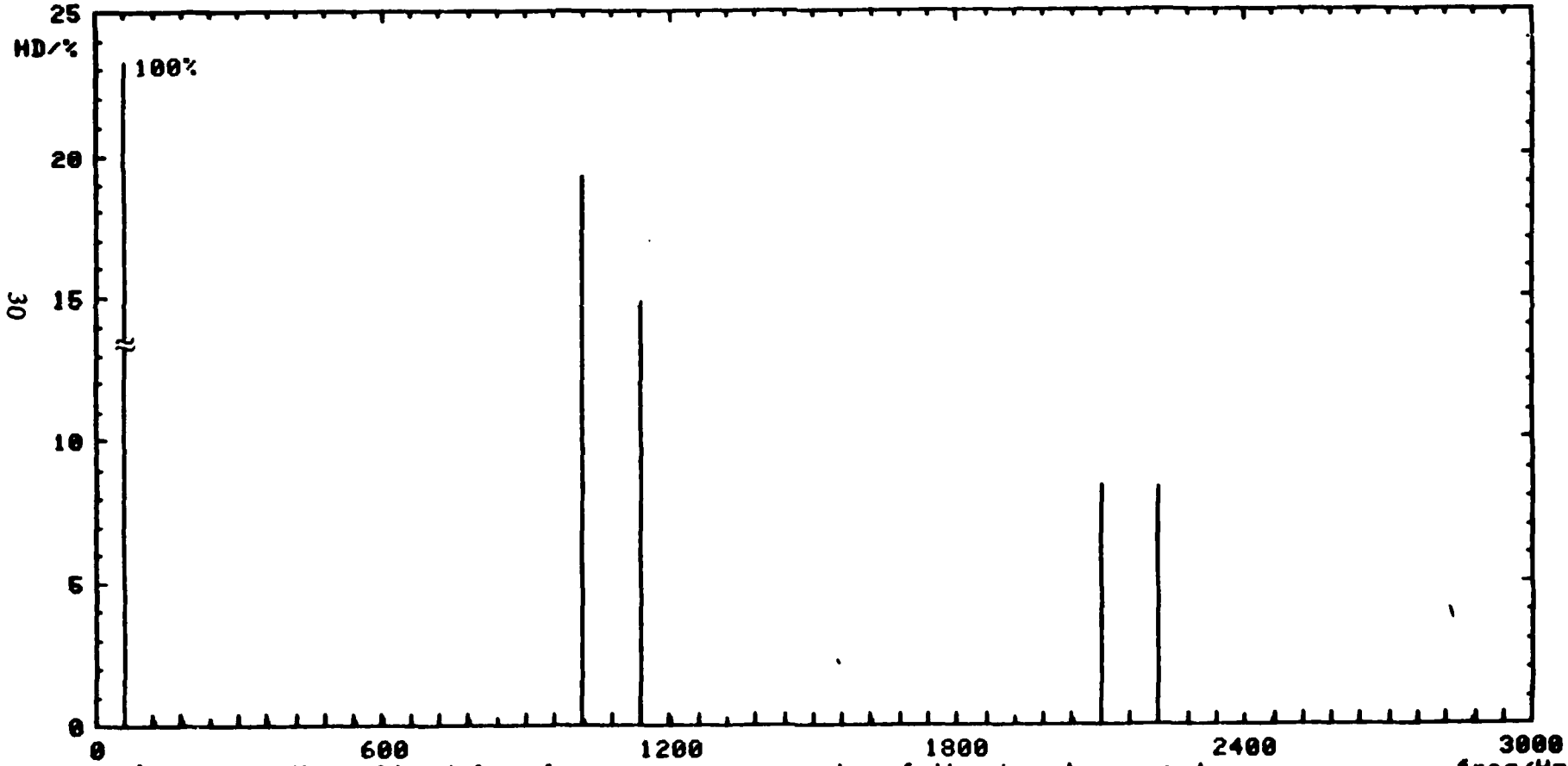

fig. 3(b) Normalized low-frequency components of the input current
(1/Ts = 25.9 KHz, fi = 60 Hz, fm = 180 Hz, m = 0.1)

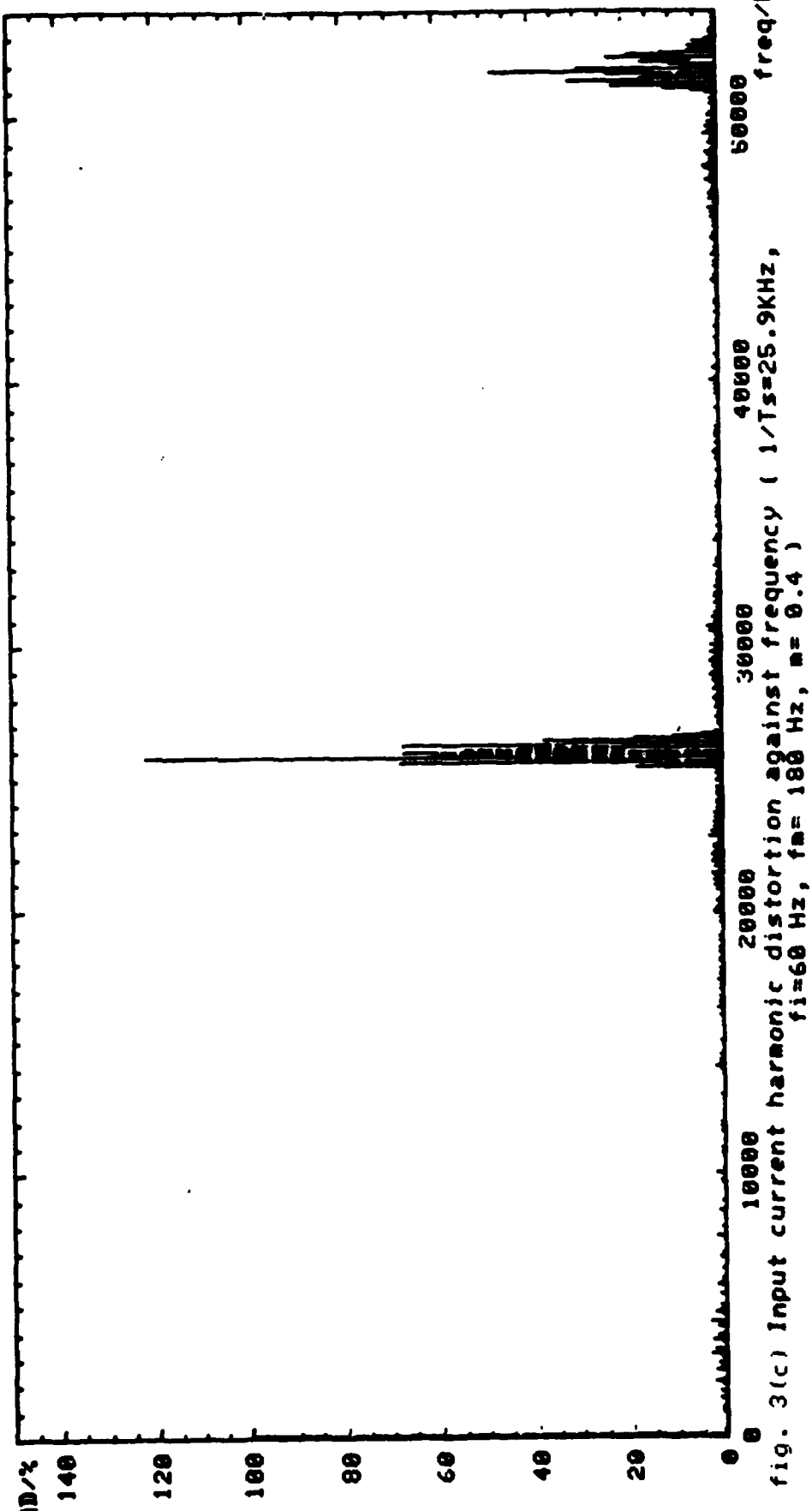

fig. 3(c) Input current harmonic distortion against frequency (1/Ts=25.9KHz, fi=60 Hz, fm= 180 Hz, m= 0.4)

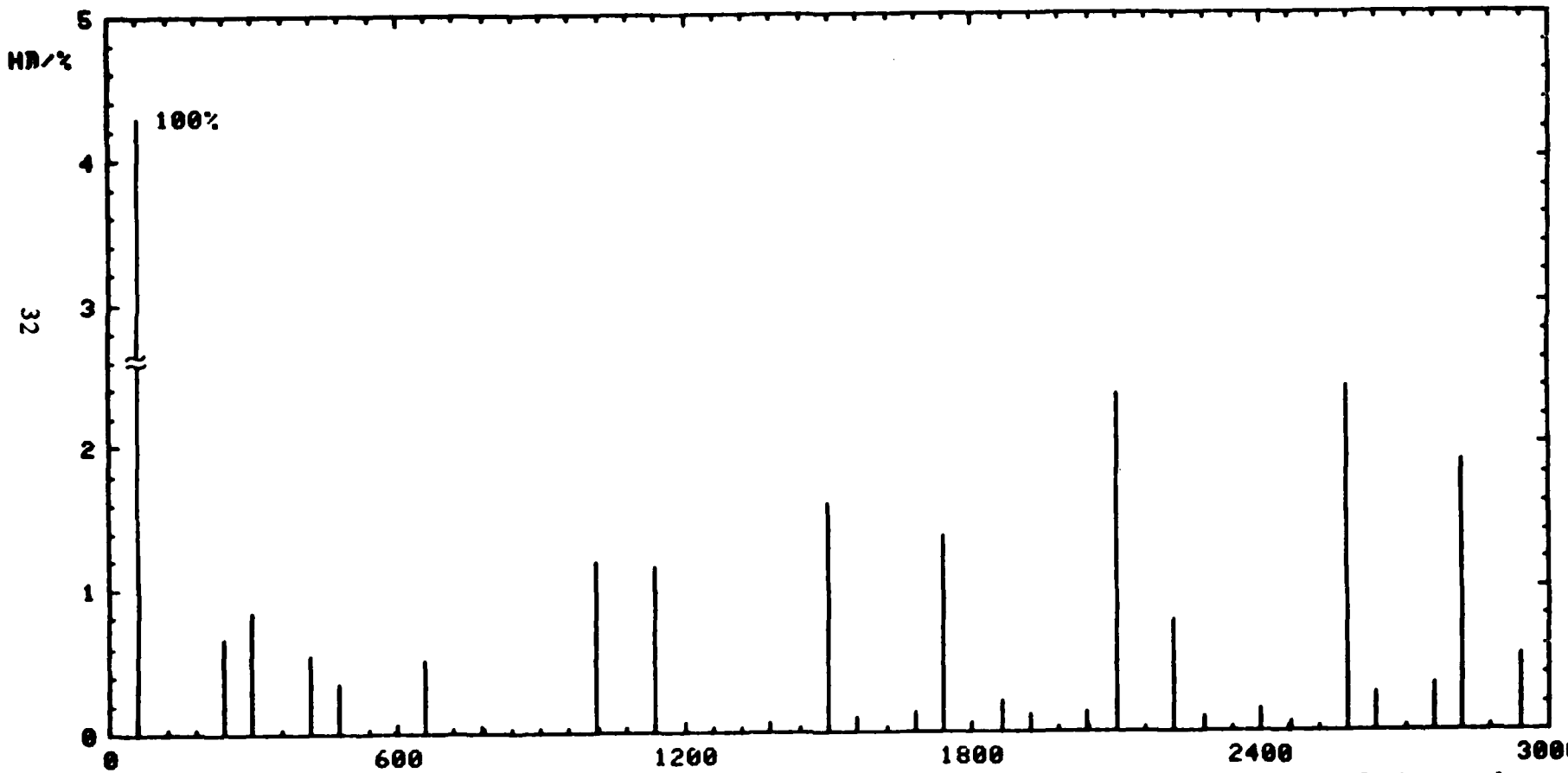

fig. 3(d) Normalized low-frequency components of the input current (1/Ts=25.9KHz, fi = 60 Hz, fm = 180 Hz, m = 0.4)

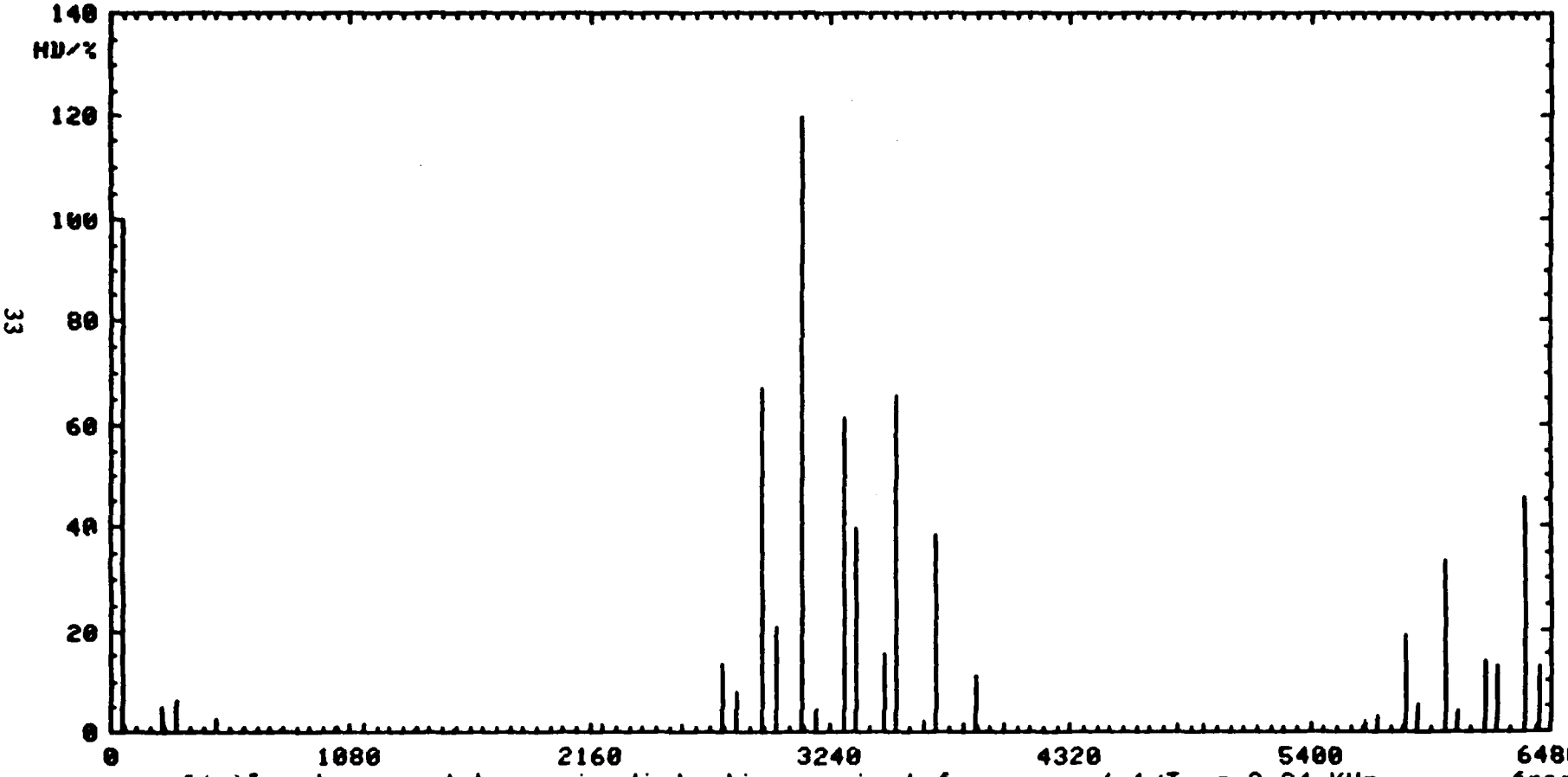

fig. 3(e) Input current harmonic distortion against frequency (1/Ts = 3.24 KHz, fi = 60 Hz, fm = 180 Hz, m = 0.4)

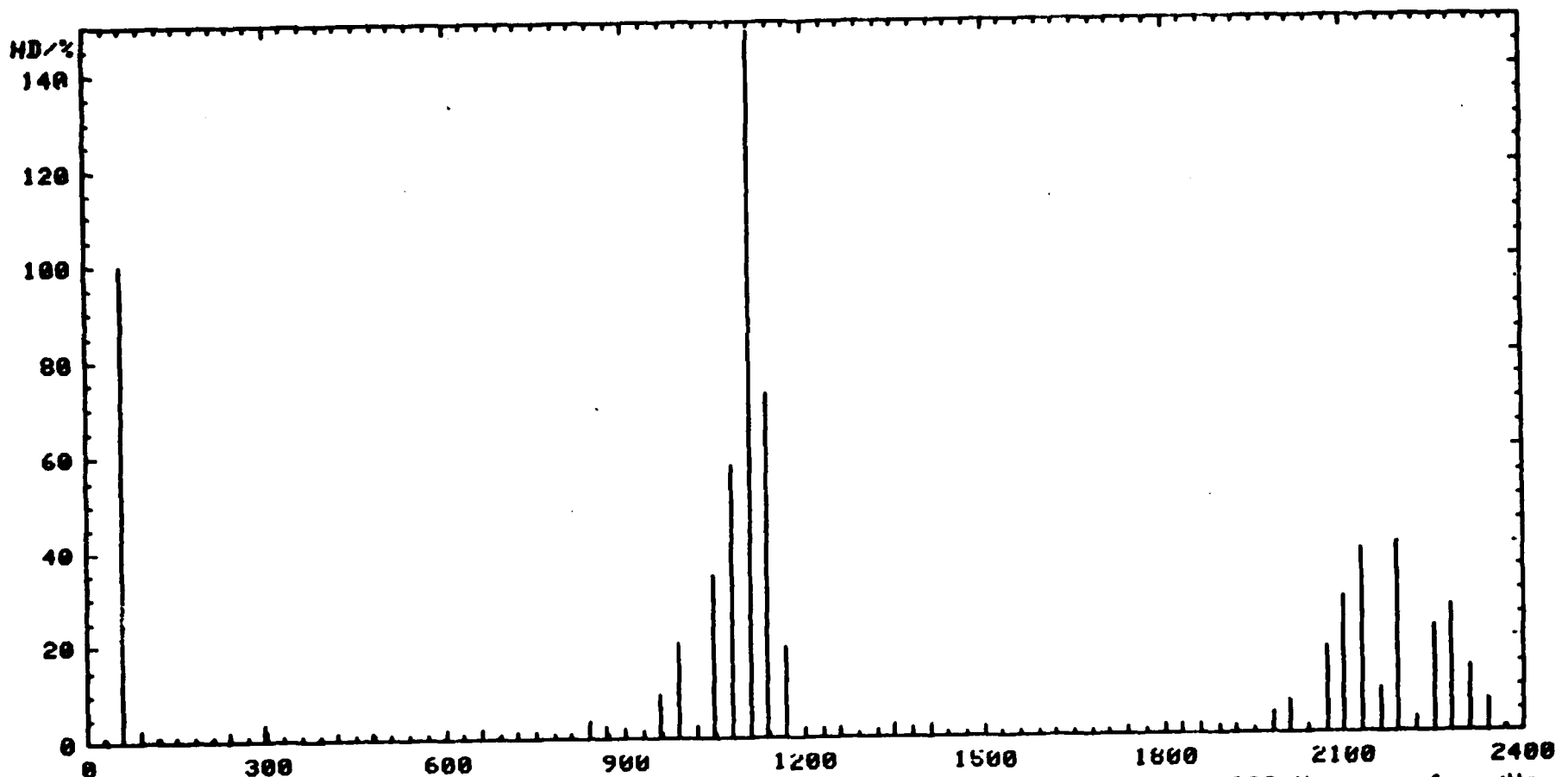

fig. 3(f) Input current harmonic distortion against frequency (1/Ts= 1080 Hz, fj = 60 Hz, fm = 30 Hz, m = 0.4)

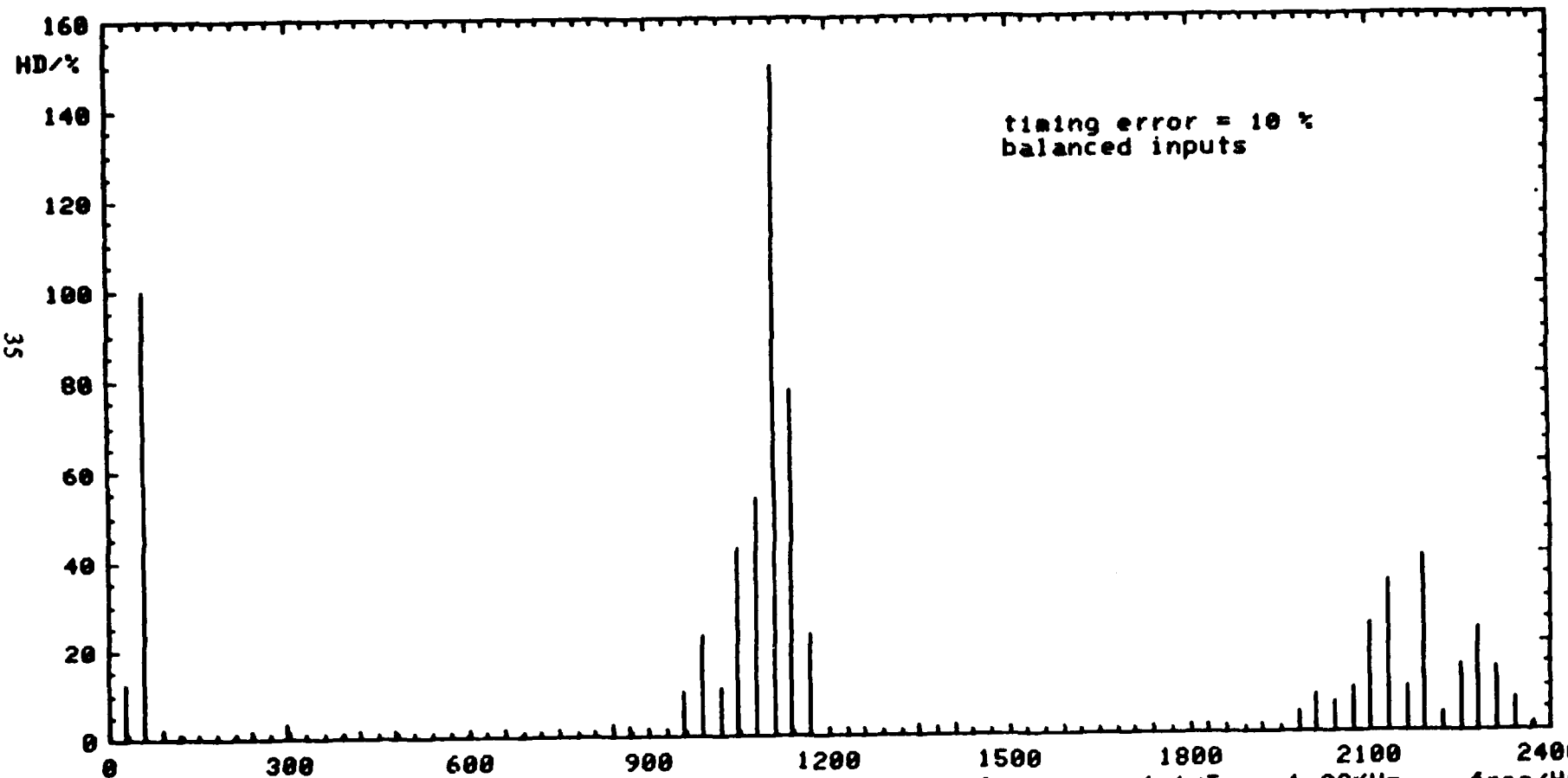

fig. 3(g) Input current harmonic distortion against frequency (1/Ts = 1.08KHz, fi = 60 Hz, fm = 30 Hz, m = 0.4)

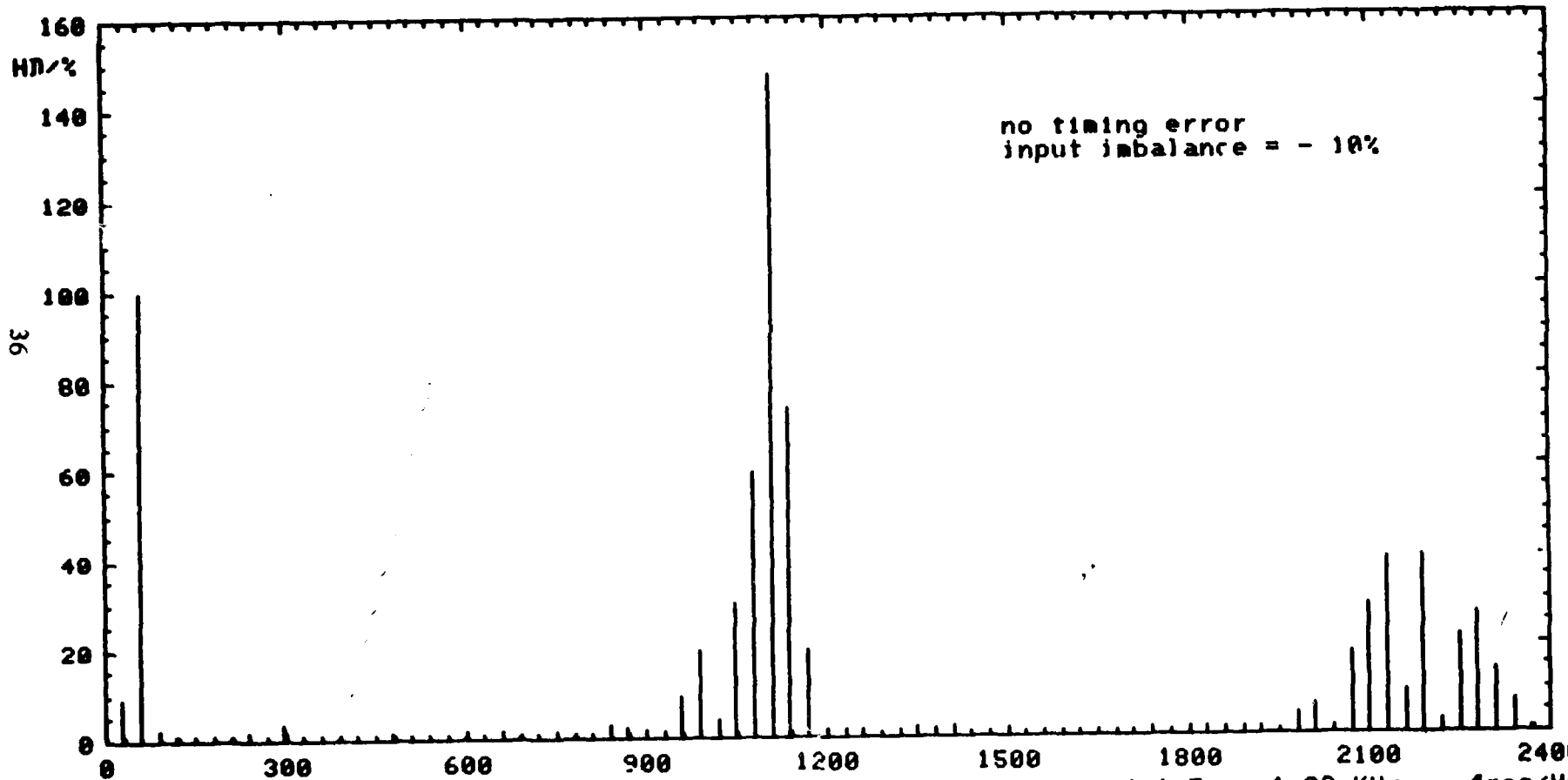

fig. 3(h) Input current harmonic distortion against frequency (1/Ts = 1.08 KHz, fi = 60 Hz, fm = 30 Hz, m = 0.4)

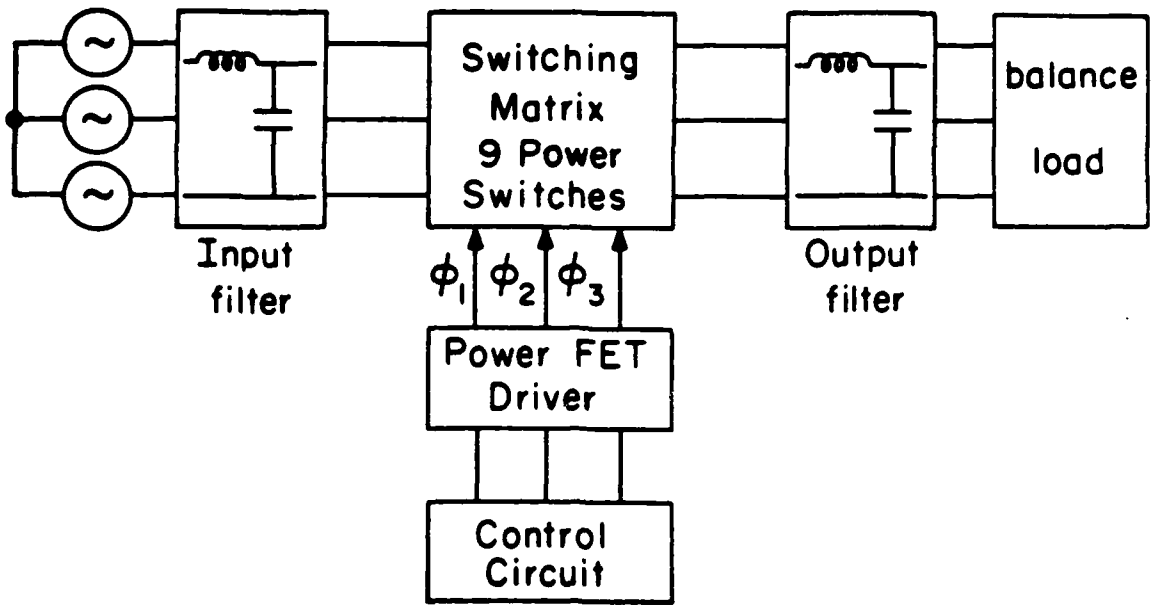

Fig. 4 Block diagram of the power converter. The filter configurations are chosen to give sinusoidal output voltage and input current. Notice that the input and the output can be reversed.

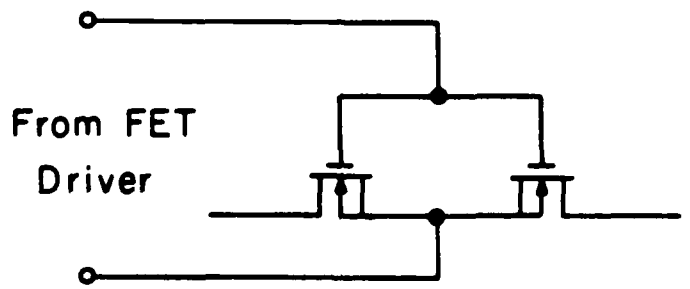

Fig. 5 Two power MOSFET's are connected in series to form a bidirectional switch. The converter uses a total of nine such switches.

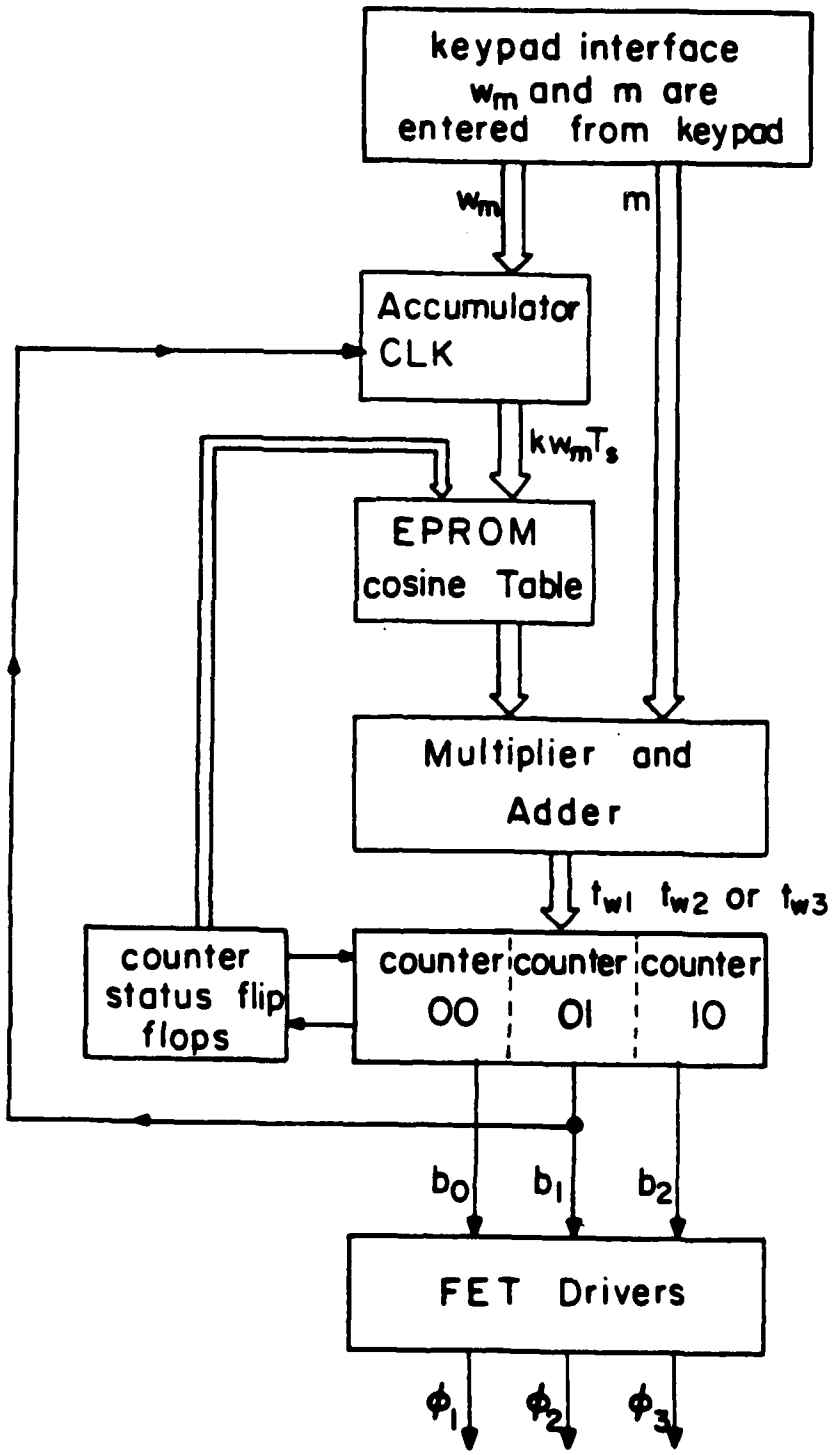

Fig. 6(a) Block diagram of the control unit used to generate the command pulses. For simplicity, an open-loop system is adopted. bo, b1 and b3 are the borrow outputs of the counters. They indicate whether the counters 00, 01 or 10 has reached zero respectively. The required pulse widths for ϕ1, ϕ2 and ϕ3 are computed by counting tw1, tw2 and tw3 to zero respectively.

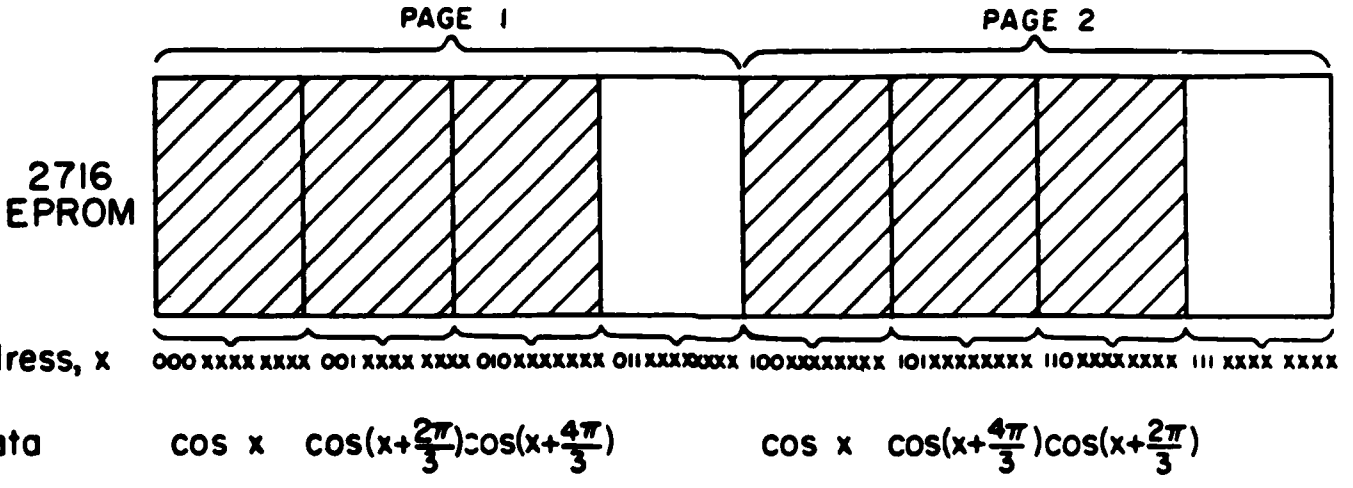

Fig. 6(b) Structure of the cosine look-up table.

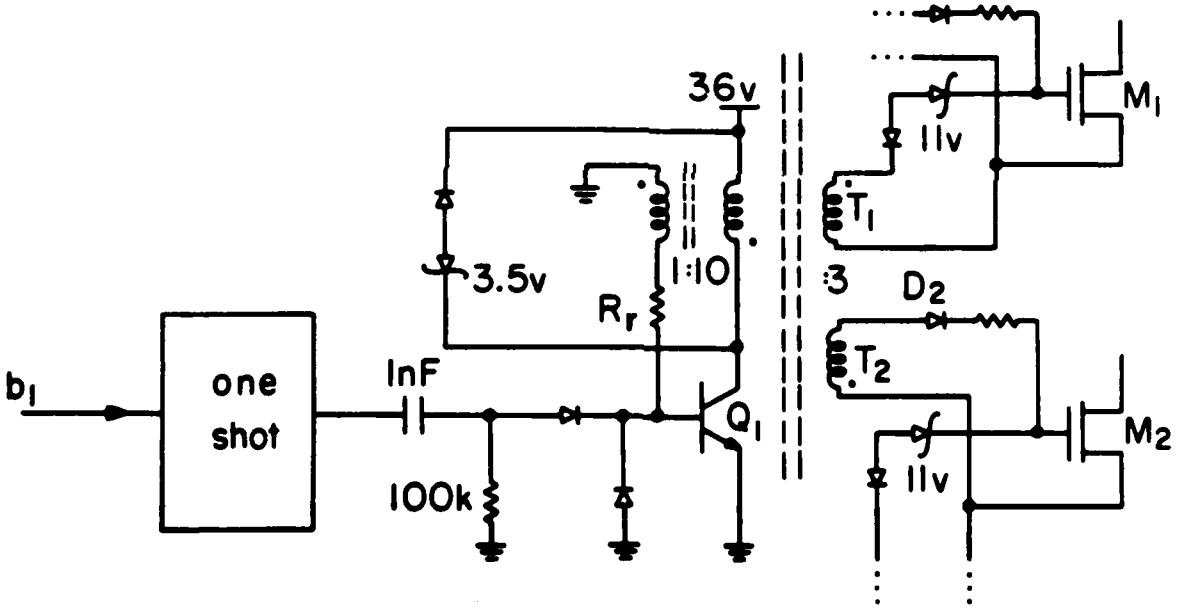

Fig. 6(c) MOSFET driver. Whenever counter O1 puts out a borrow pulse, the set of three which were on should be turned off and another set should be turned on. Here the b1 pulse causes Q1 to saturate and turns on M2 through T2. Meanwhile M1 is turned off through T1. The gate-source voltage of M2 is maintained by D2 after Q1 comes out of saturation. An important consequence is that the on-times of M1 and M2 overlap.

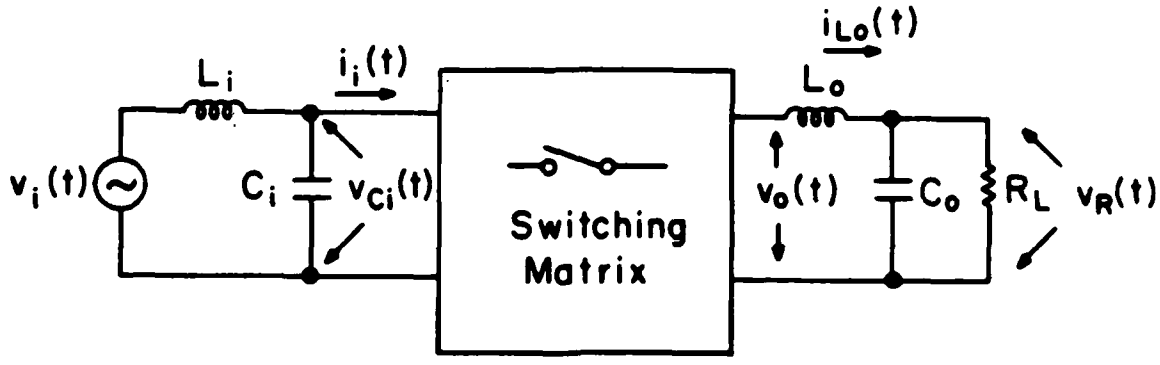

Fig. 7 One possible filter configuration for switching power converter. Because of the bidirectional property of the converter, the input and the load can be exchanged.

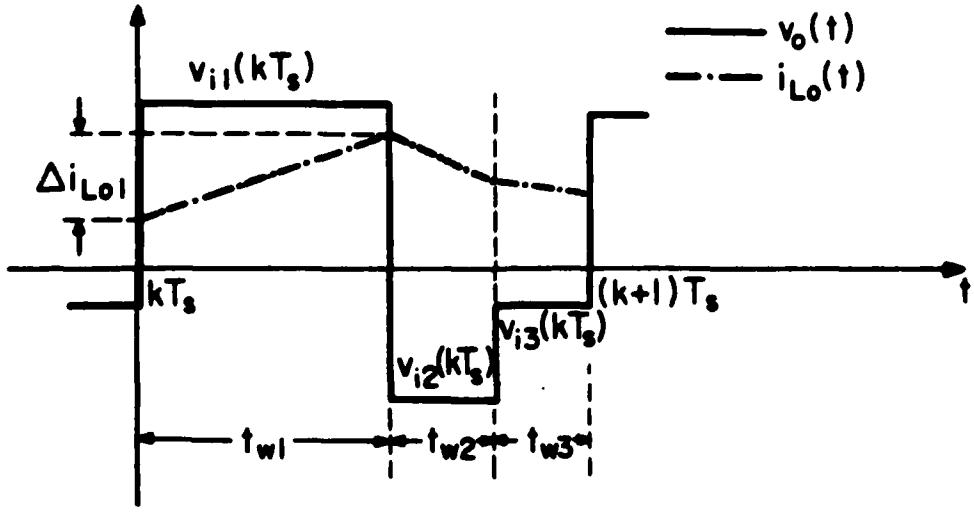

Fig. 8(a) Approximate instantaneous output voltage and output inductor current waveforms.

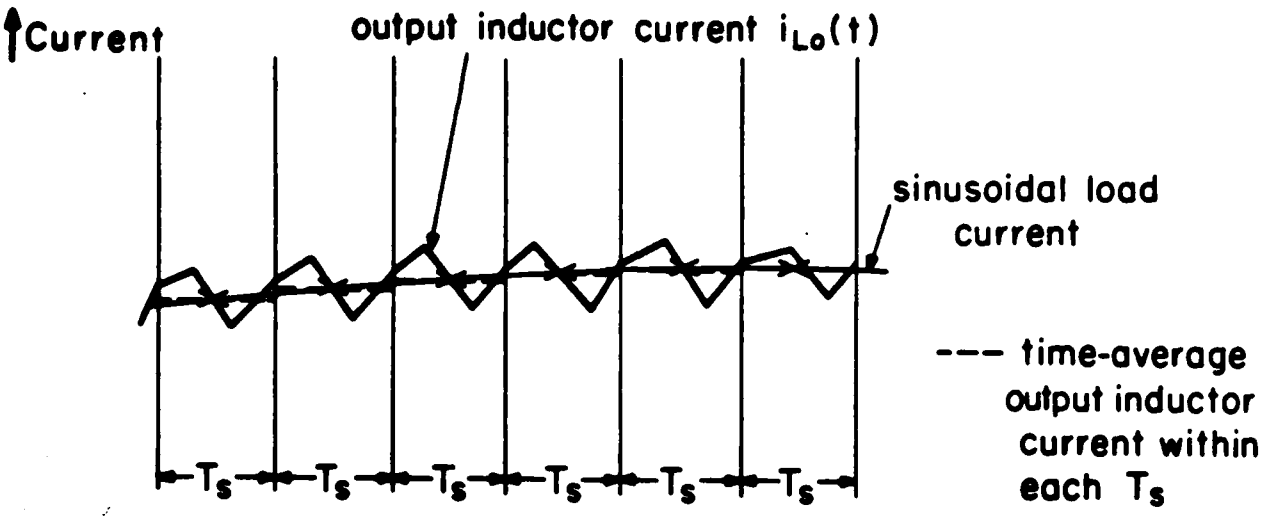

Fig. 8(b) The relationship between the load current and the output inductor current is illustrated on a magnified time scale. (the output capacitor current is neglected)

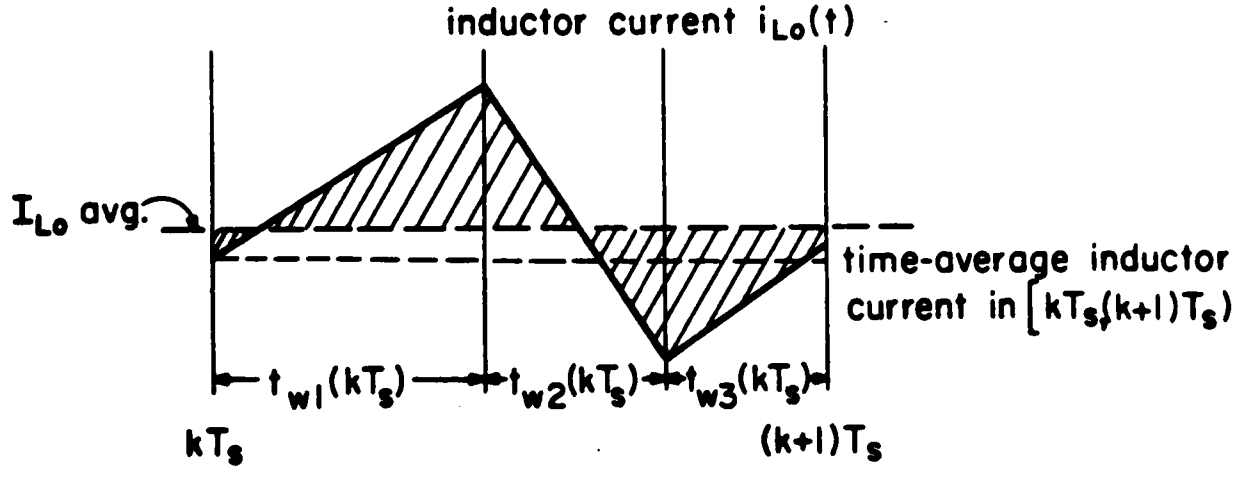

Fig. 8(c) Charge packets flowing into or out of Co are represented by the shaded areas. Therefore they are a measure of the output ripple voltage.

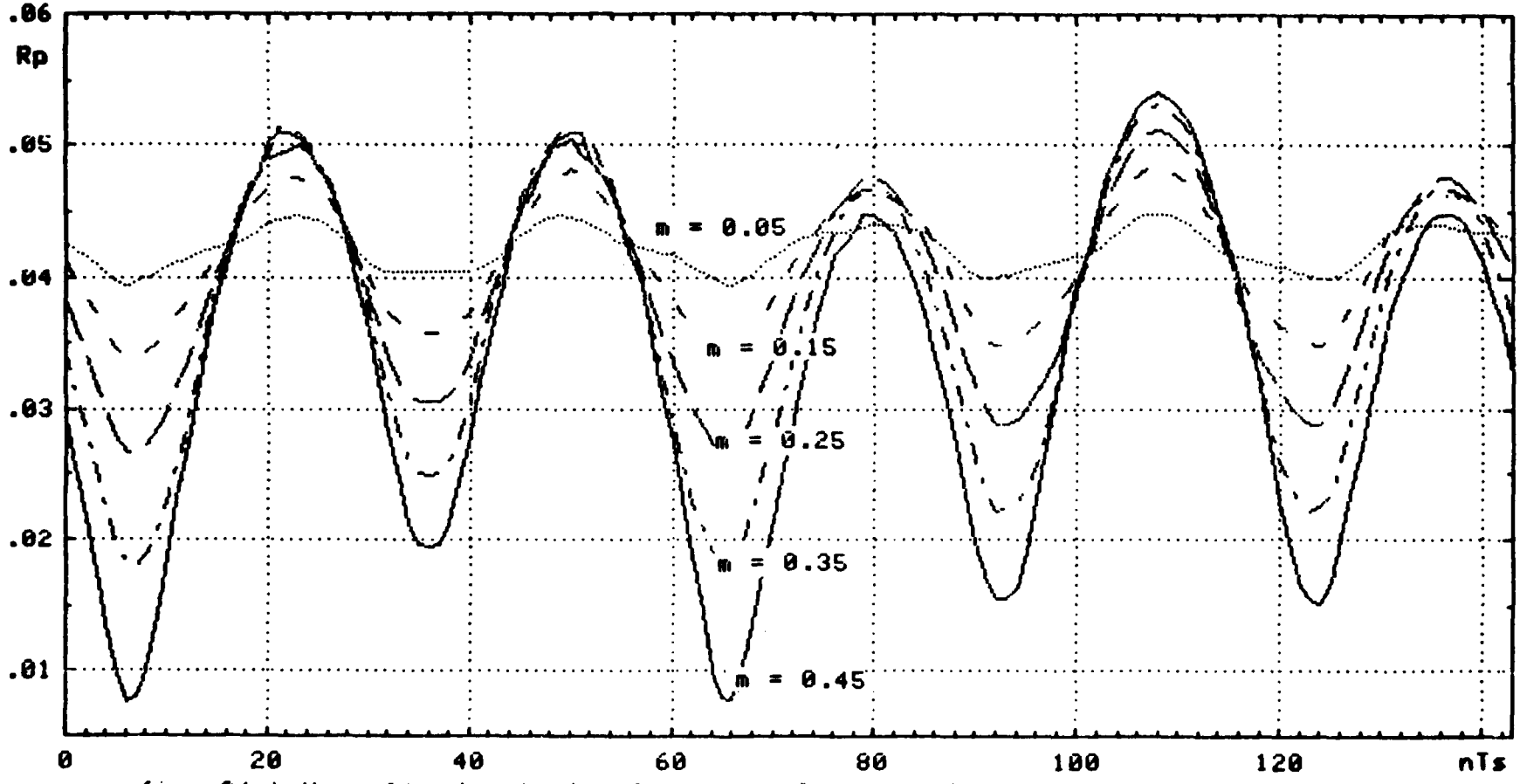

fig. 9(a) Normalized output voltage ripple against time with m as a parameter
(fi = 50 Hz, fm = 25 Hz)

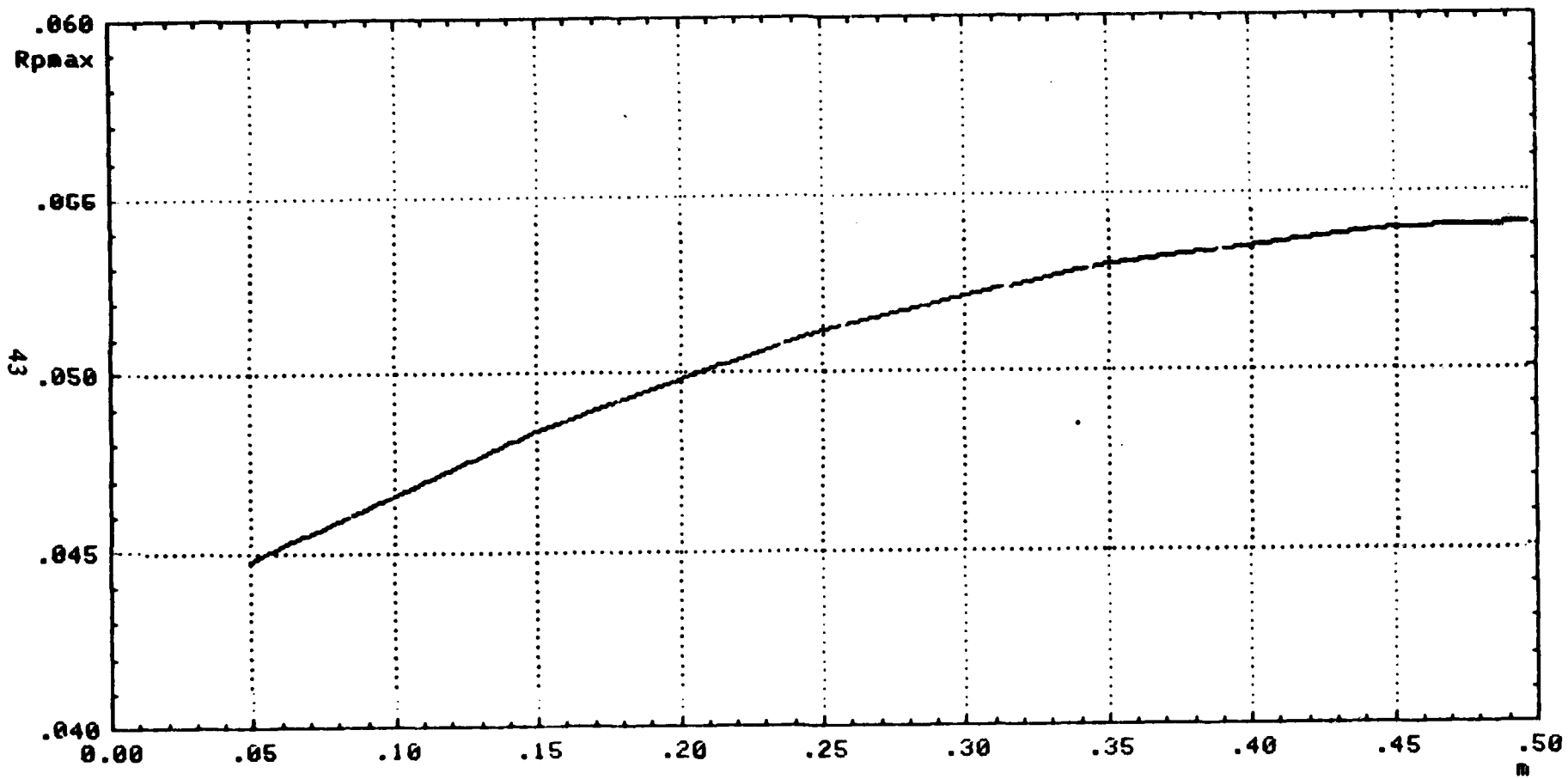

fig. 9(b). Maximum normalized output volatge ripple against m (fi=50Hz, fm=25 Hz)

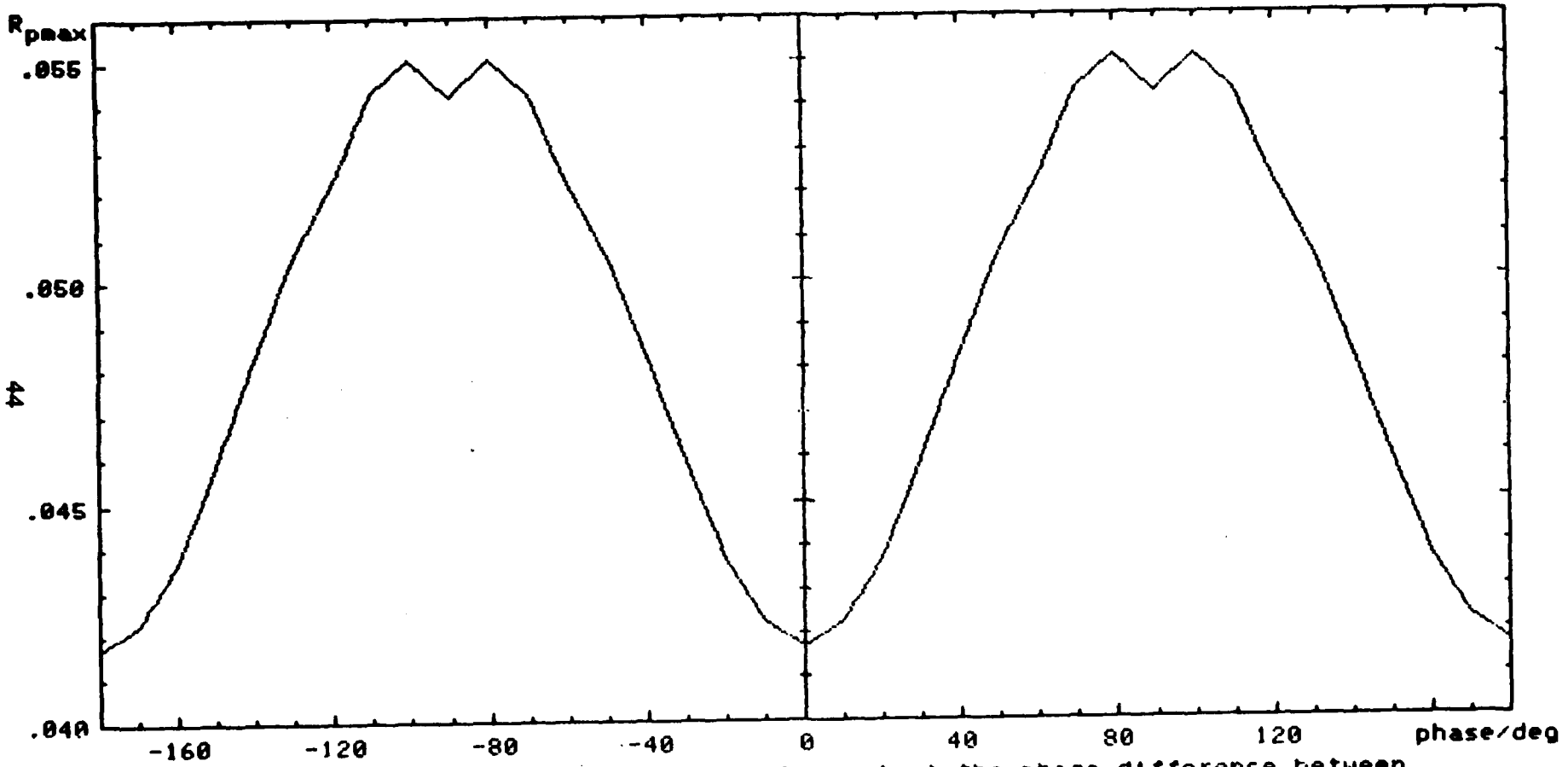

fig.9(c) Maximum normalized voltage ripple against the phase difference between the input and modulating waveforms (fi=100 Hz, fm=100 Hz, m=0.5)

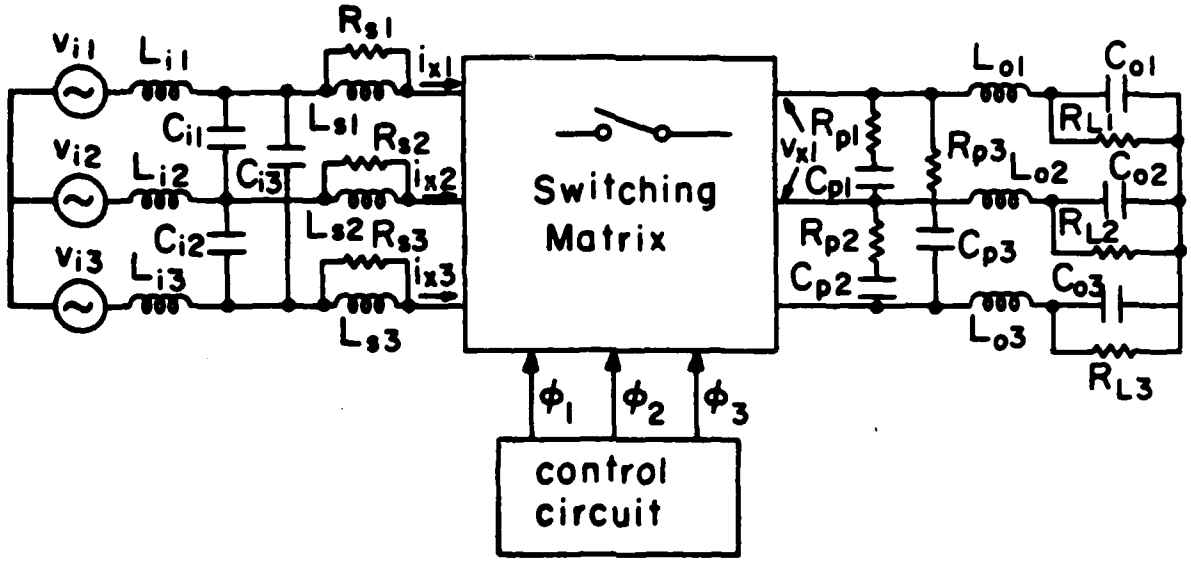

fig. 10 Complete power converter with filters and protection.

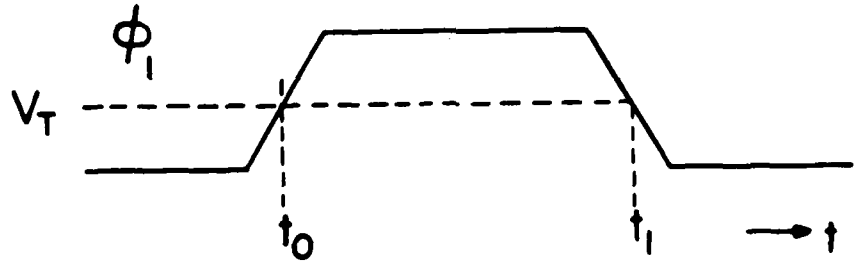

Fig. 11 Control pulse ø1 on an expanded time axis. VT denotes the threshold voltage of the MOS power FET's. S11, S22 and S33 are closed during (t0, t1).

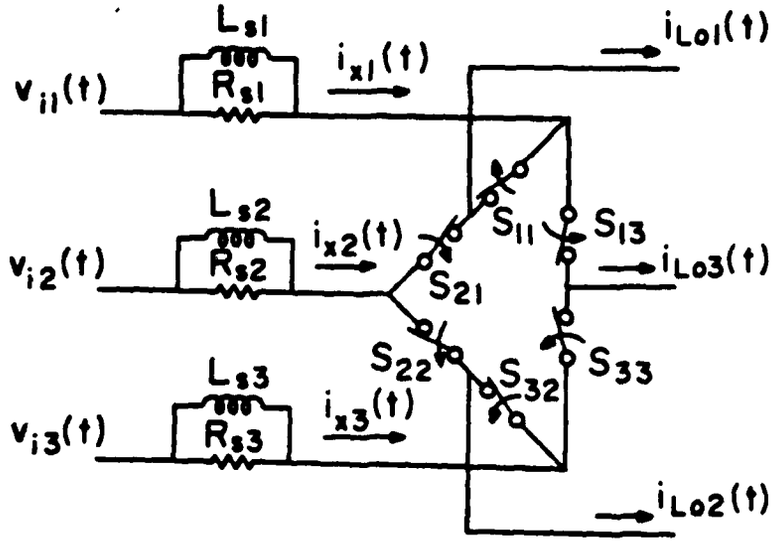

Fig. 12 Circuit schematic of the three-phase short circuit formed during switching exchange between the groups {S11, S22, S33} and {S21, S32, S13}.

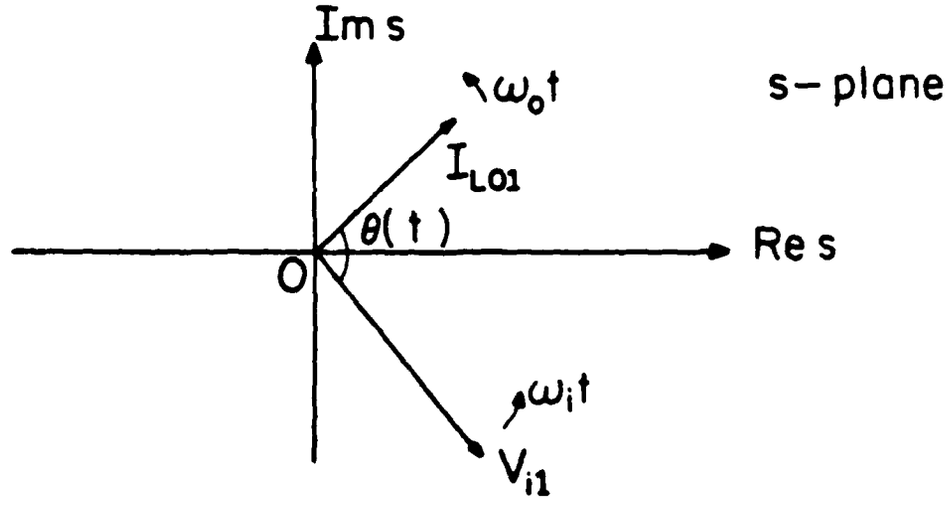

Fig. 13 The maximum switch current occurs when the rotating vectors ILo1 and Vi1 both fall on the positive axes.

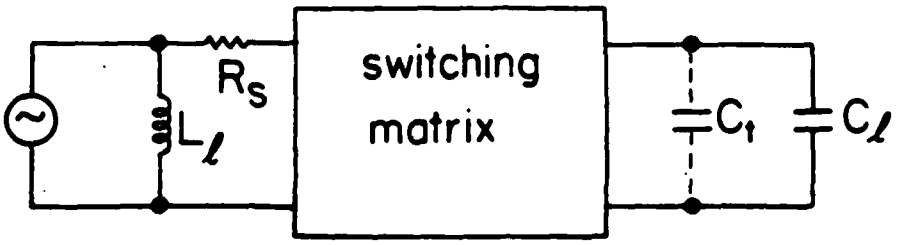

Fig. 15 Lumped parasitics L1 and C1 are calculated with test capacitor Ct.

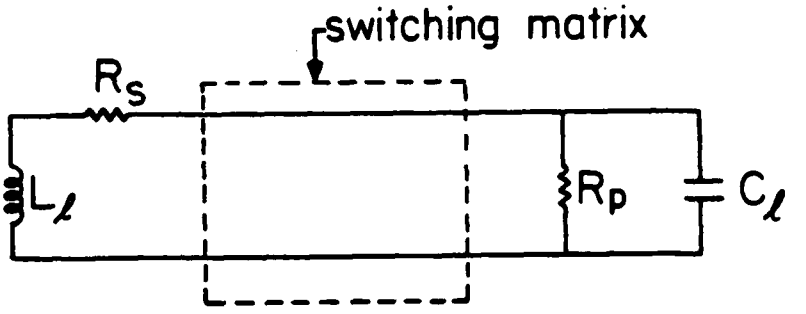

Fig. 16 The equivalent parasitic RLC circuit. Increased damping is achieved with the inclusion of Rp.

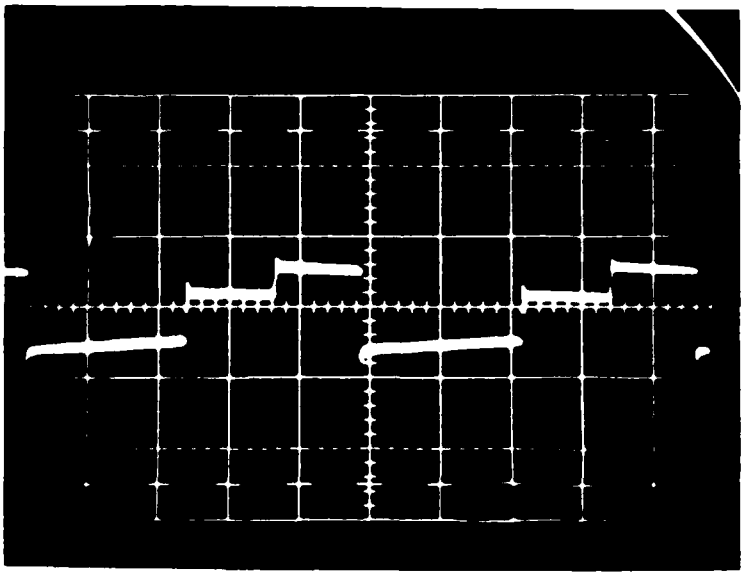

Fig. 14(a) vx waveform (dc-ac conversion, 50 V/div, 20 us/div).

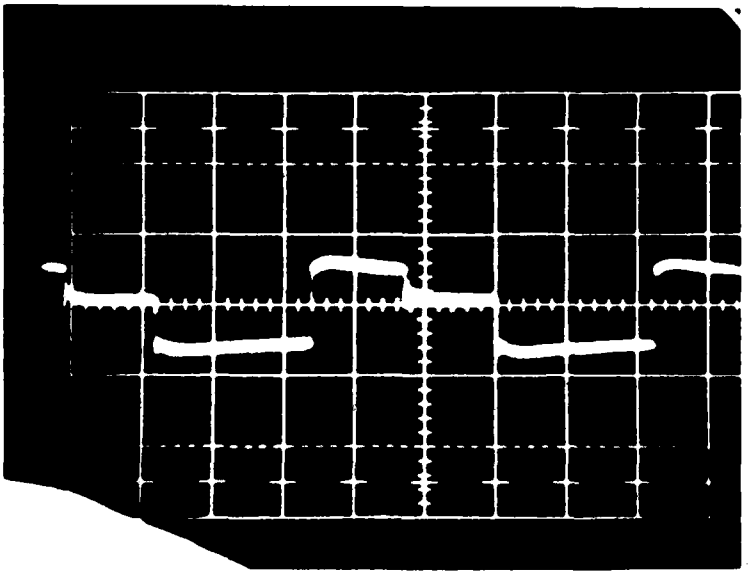

Fig. 14(b) vx waveform (dc-ac conversion) with damping resistor Rp=300 ohms. (50 V/div, 20 us/div)

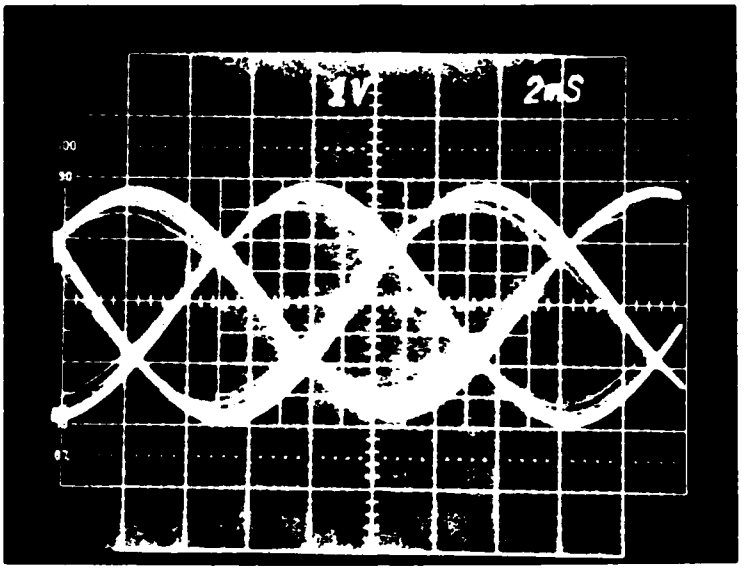

Fig. 17(a) Unfiltered output voltage vx1.

Operating Condition : m = 0.2, Ts = 72 us, Vi = 17V line-to-line, Co = 5 uF, Lo = 0.2 H, Ci = 3 uF, Li = 0.1 H, RL = 100 ohms, Rs = 30 ohms, Rp = 330 ohms, Cp = 10 nF.

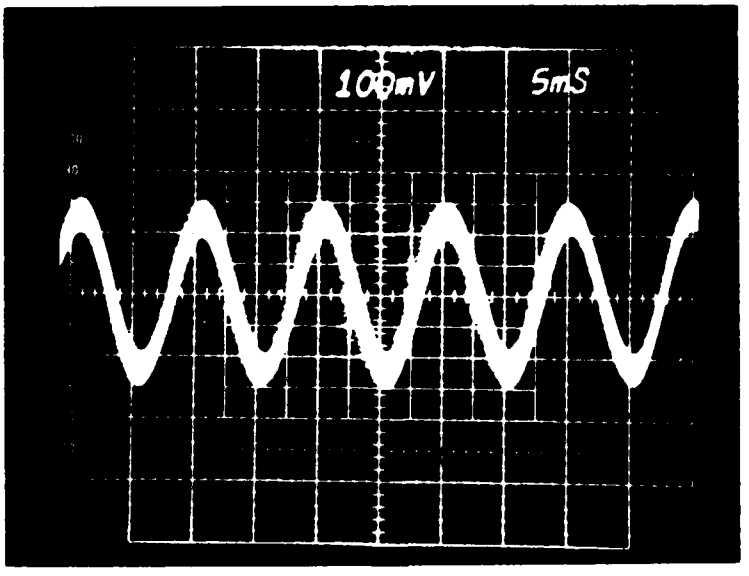

Fig. 17(b) Filtered output voltage vR1.

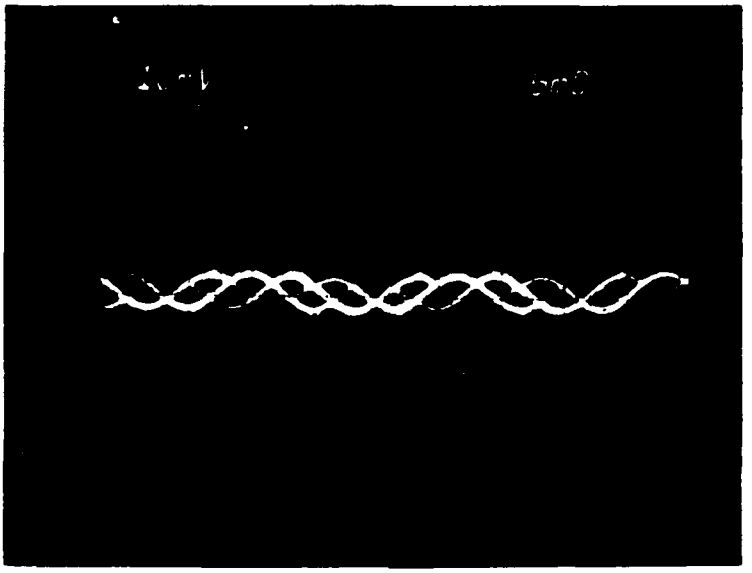

Fig. 17(c) Unfiltered input current ix1 (50mA/div).

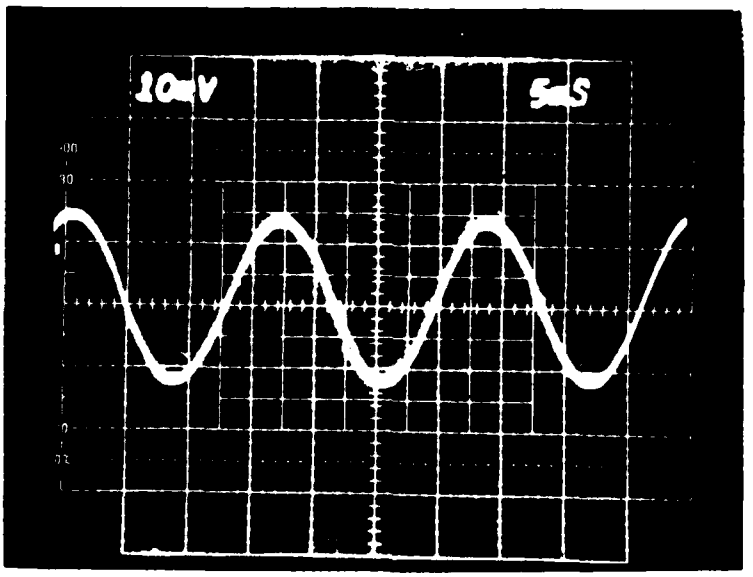

Fig. 17(d) Line current iin1 (25mA/div).

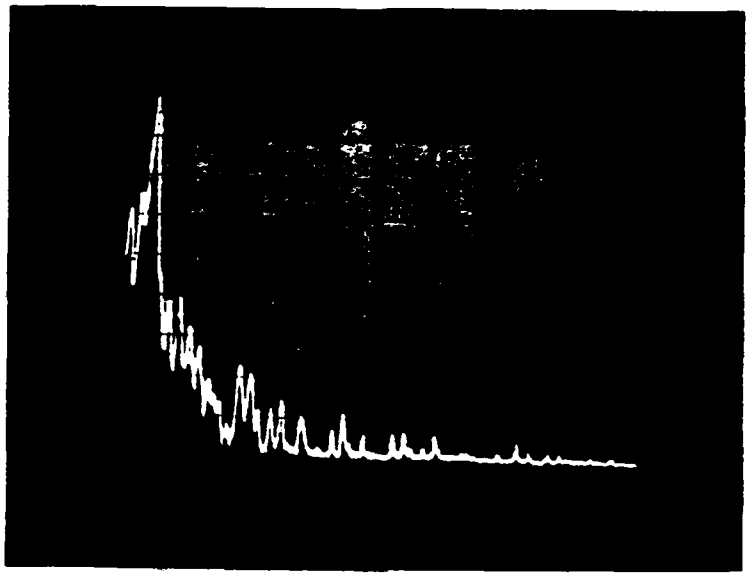

Fig. 17(e) vR1 spectrum (10db/div, 200Hz/div).

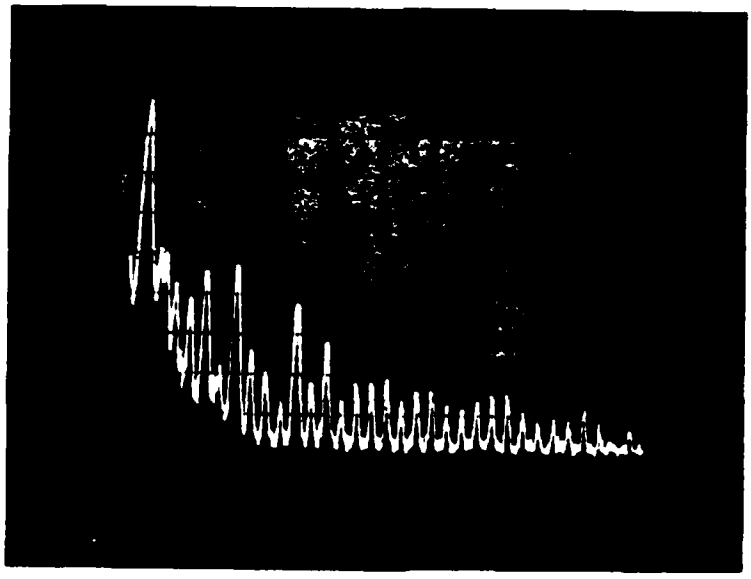

Fig. 17(f) iin1 spectrum (10db/div, 200Hz/div).

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